

CONTENT	SHEET
Cover Sheet, Block diagram	1-2
Intel LGA775 CPU - Signals	3-5
Intel Bearlake - FSB, PCIE, DMI, VGA, MSIC	6
Intel Bearlake - Memory DDR2	7
Intel Bearlake - Power / GND	8-9
ICH9 - PCI, USB, DMI, PCIE	10
ICH9 - Host, DMI, SATA, Audio, SPI, RTC, MSIC	11
ICH9 - Power, GND	12
DDR2 Channel-1 / Channel-2	13-14
SLG84516BT CLK Gen.	15
SCH5617, COM1,2, FDD	16
CPU/SYS/PWR FAN	17
PCI-Express x16 & x1	18
PCI Slot	19
USB CONNECTOR	20
ATX ,Front Panel & VGA Connector	21
KB/MS/TPM/PARALLEL	22
VRD11 Intersil 6312 3Phase	23
MS7 ACPI Controller	24
SATA&V_1P25_CORE	25
Broadcom-BCM5787M	26
LAN-NINEVEH 82566	27
HD Audio ALC262	28
GPIO & Jumper setting	29
MANUAL PARTS	30
POWER Distribution	31
PWROK MAP	32
RESET MAP	33
History	34

NEC:ROPROS

MS-7410 uATX

Version: 0B



CPU: Intel, Socket 775 (Intel Core 2 Duo Processors, Intel Pentium D Processors, Intel Pentium 4 Processors, Intel Celeron D Processors)--
65-95 watts Intel Core 2 Duo, Pentium D, Celeron D

System Chipset:

Intel Bearlake - Q (North Bridge)

Intel ICH9 Series (South Bridge)

ROPROS-MA use ICH9 / ROPROS-VS use ICH9DH / ROPROS-NECCAP use ICH9R

On Board Device:

CLOCK Gen -- SLG84516BT CLK Gen.

LPC Super I/O -- SCH5617

LAN -- Broadcom-BCM5787M

LAN -- INTEL 82566 (Support ViiV)

HD Audio Codec -- ALC262 VER:C2

TPM - SLB9635

How to distinguish the different SKU

Main Memory:

Dual-channel DDR-II * 4

Expansion Slots:

PCI EXPRESS X16 SLOT * 1

PCI EXPRESS X1 SLOT * 1

PCI SLOT * 2

PWM: VRD11 Intersil 6312 3Phase

	BLUE Color which mean all model need use
	SKY BLUE Color which mean ROPROS-MA/NECCAP use
	ORANGE Color which mean ROPROS-MA use
	PINK Color which mean ROPROS-VS
	GREEN Color which mean ROPROS-NECCAP
	BROWN Color which mean the part reserve

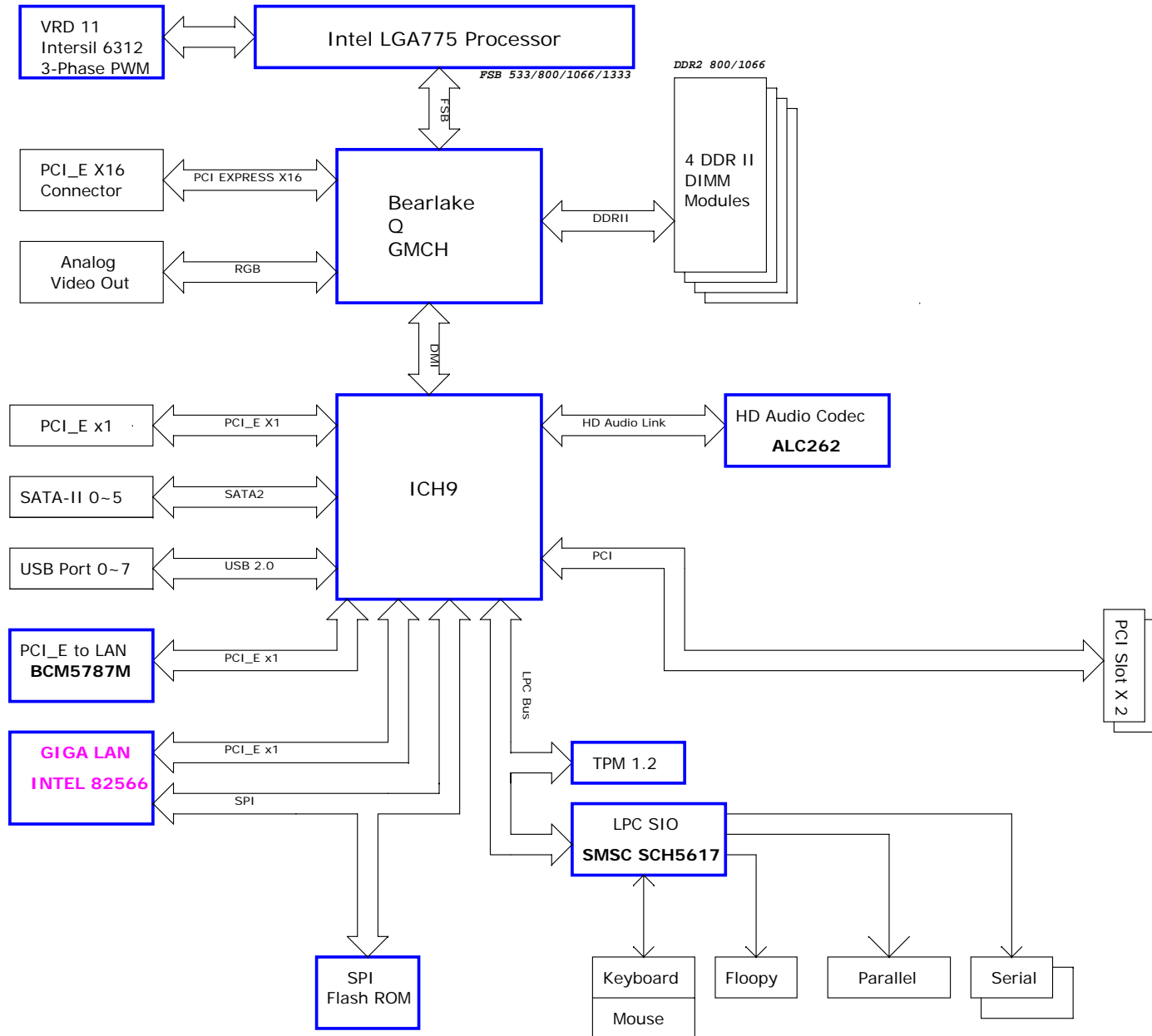


MICRO-STAR INT'L CO.,LTD

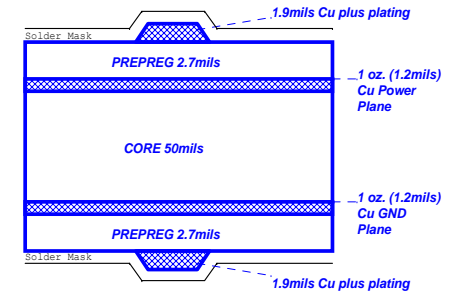
MS-7410

Size Custom	Document Description COVER SHEET	Rev 0B
Date: Wednesday, September 26, 2007	Sheet 1 of 34	

Block Diagram



Board Stack-up (1080 Prepreg Considerations)



Single End 50ohm Top/Bottom : 4mils
 USB2.0 - 90ohm : 15/7.5/4.5/7.5/15
 SATA - 95ohm : 15/8/4/8/15
 LAN - 100ohm : 15/10/4/10/15
 PCIe - 95ohm : 15/8/4/8/15

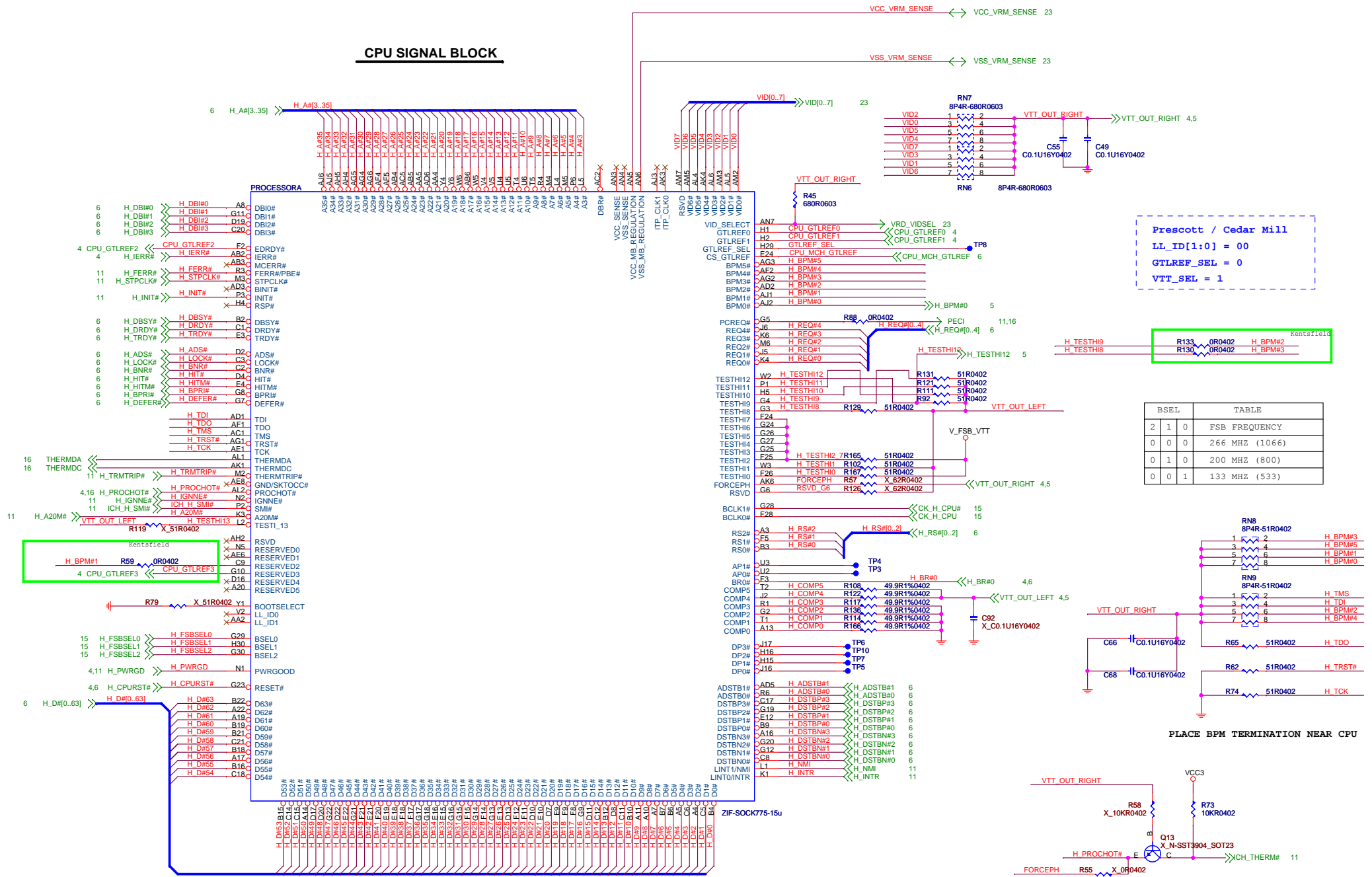


MICRO-STAR INT'L CO.,LTD

MS-7410

Size	Document Description	Rev
Custom	BLOCK DIAGRAM	0B
Date: Wednesday, September 26, 2007	Sheet 2 of 34	

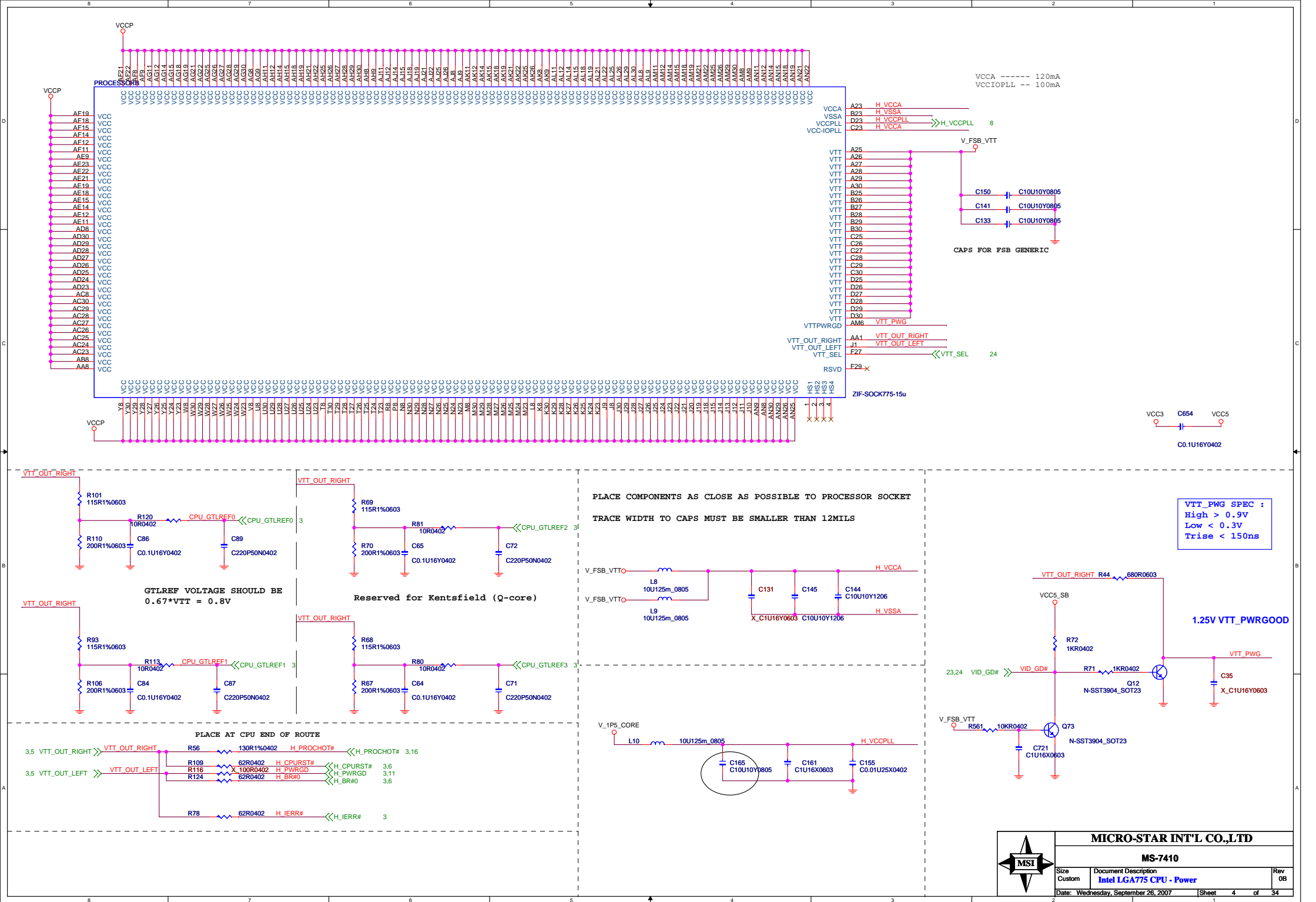
CPU SIGNAL BLOCK

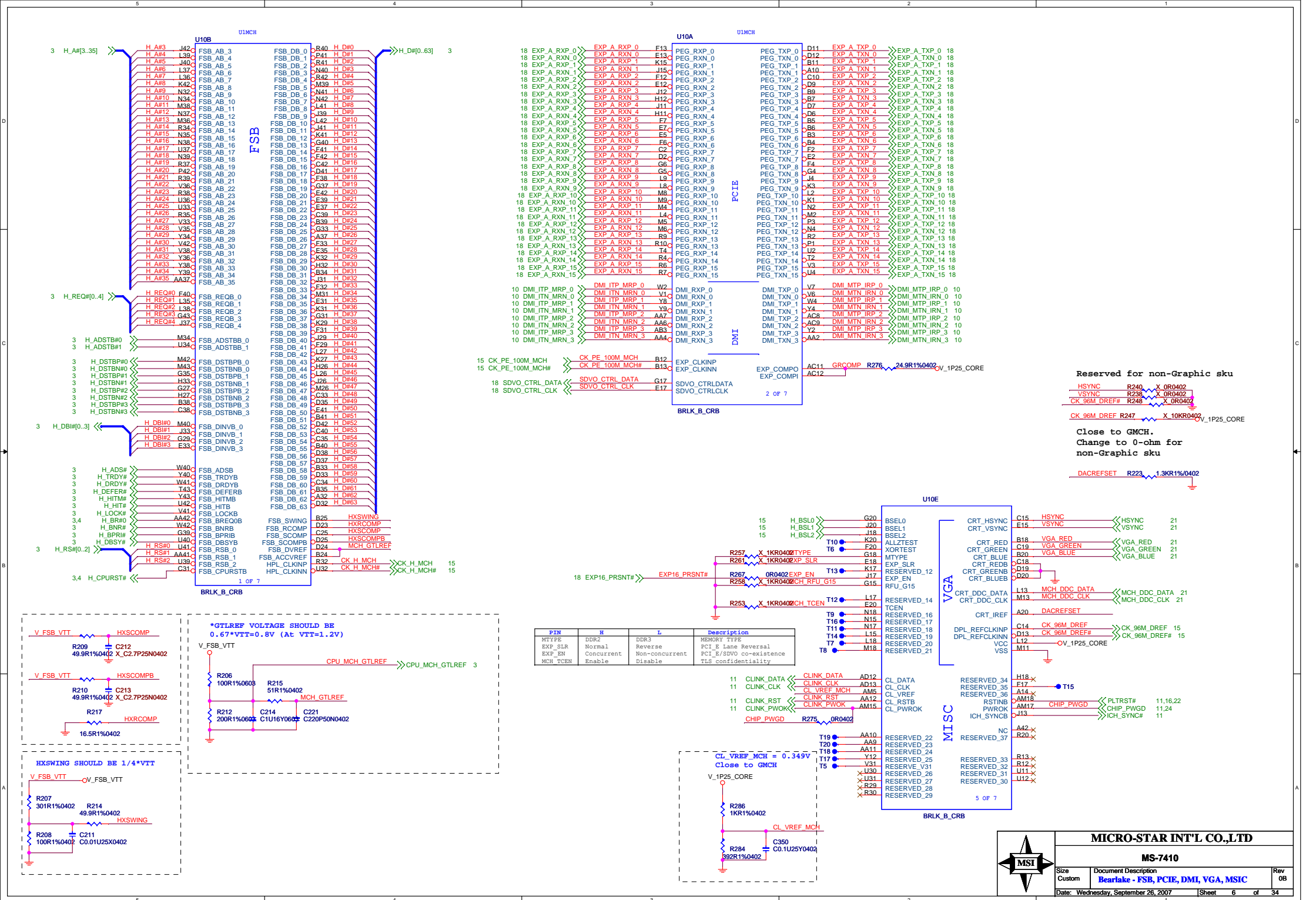


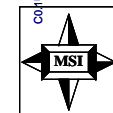
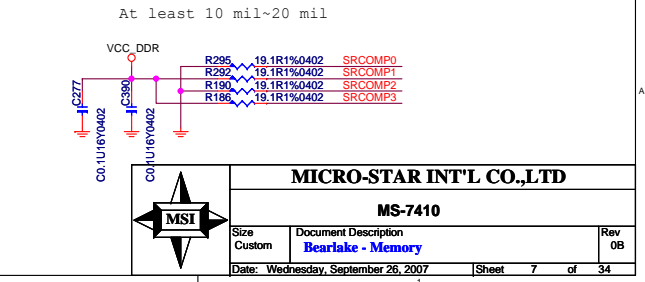
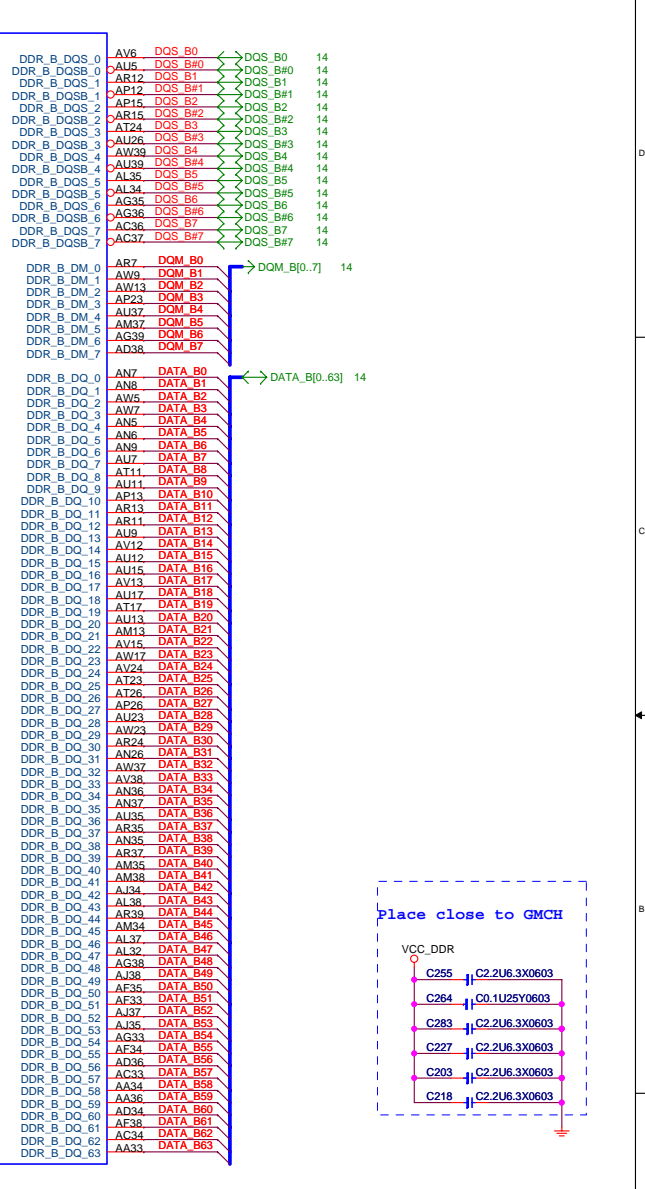
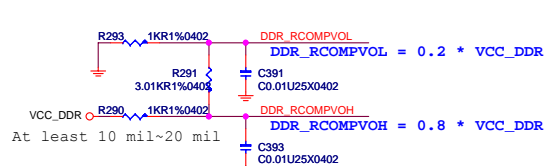
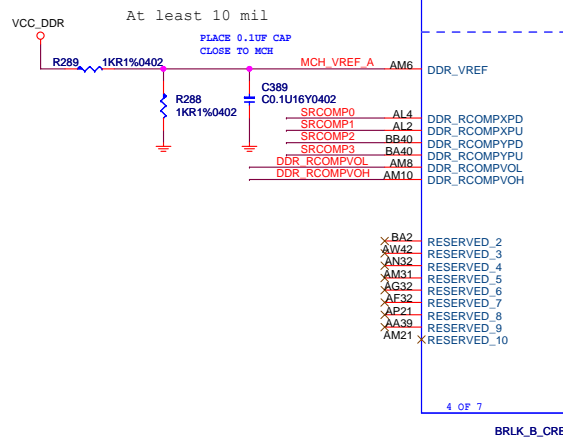
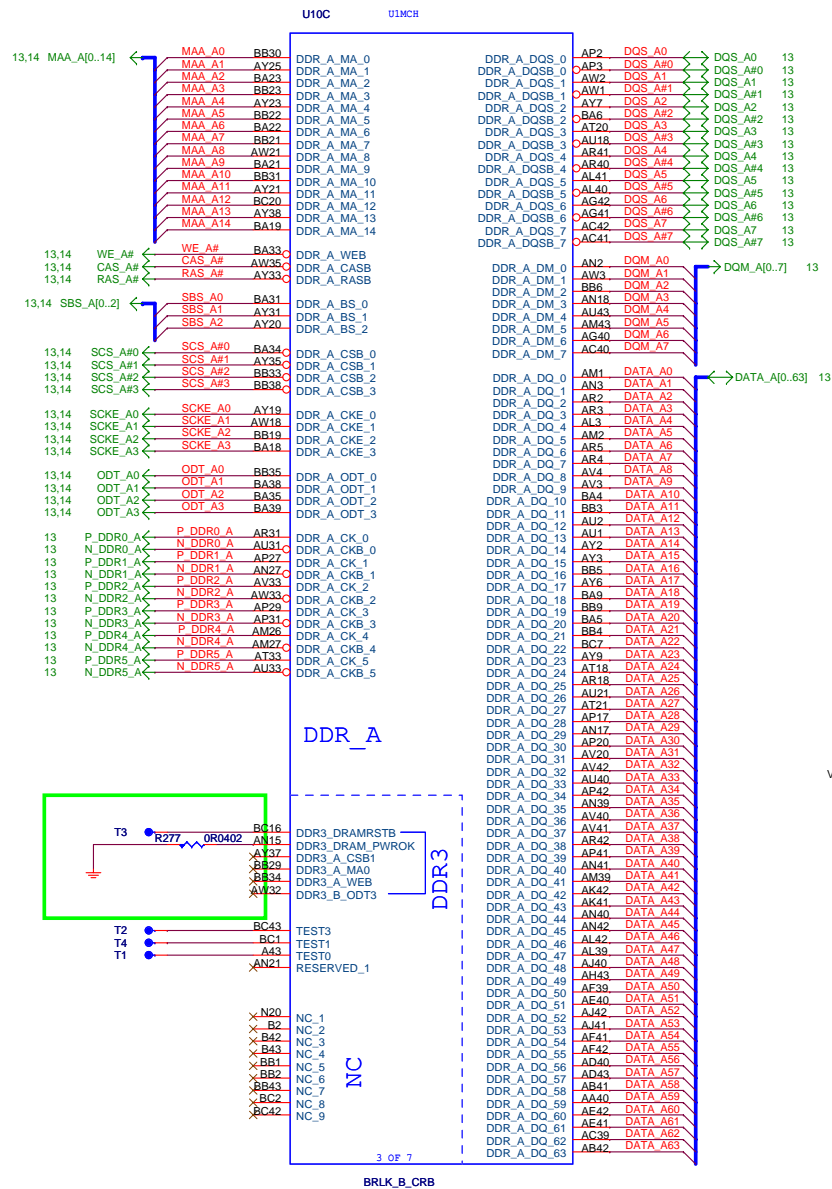
MICRO-STAR INT'L CO.,LTD

MS-7410

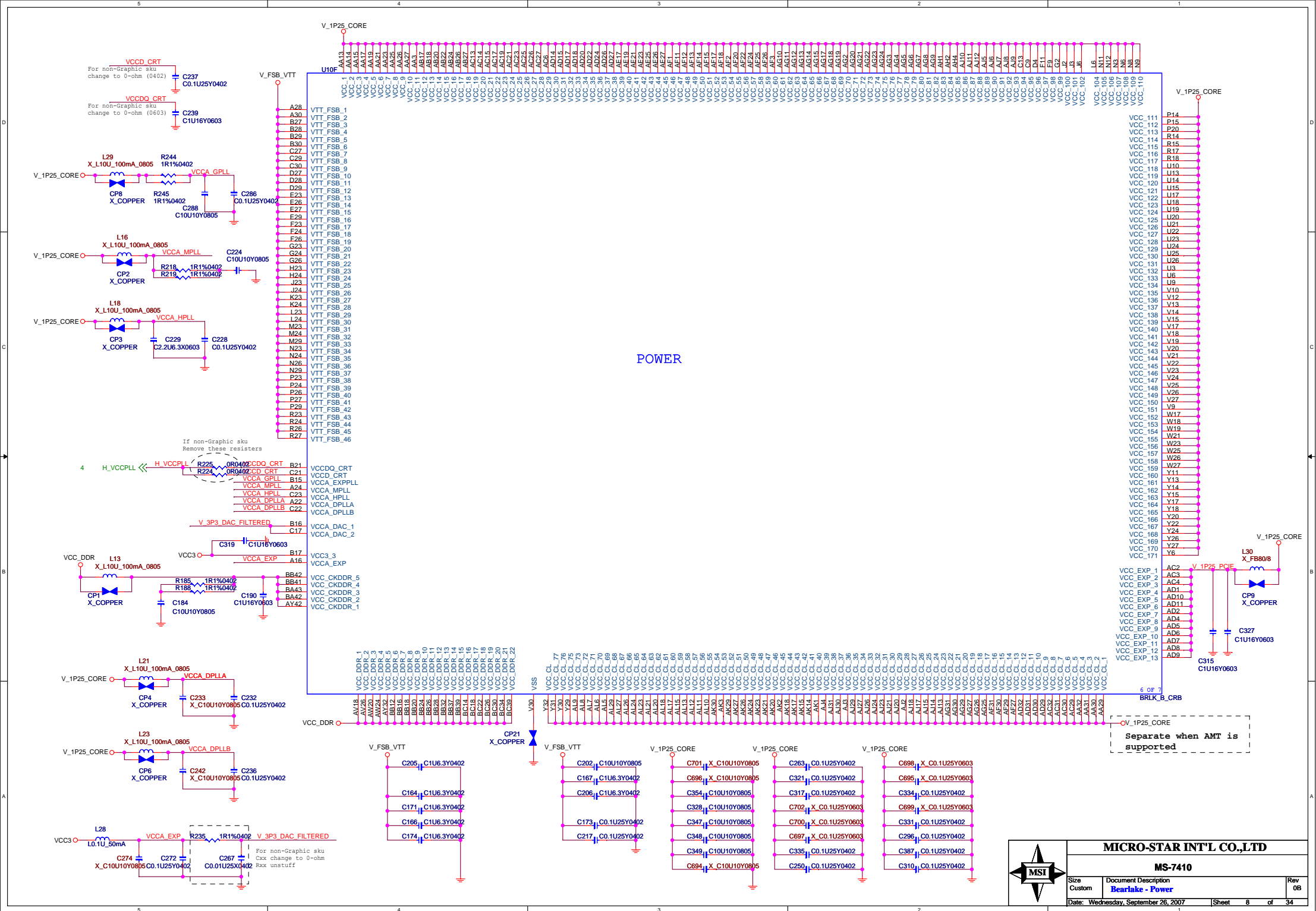
Size Custom	Document Description Intel LGA775 - Signals	Rev 0B
Date: Wednesday, September 26, 2007		Sheet 3 of 34

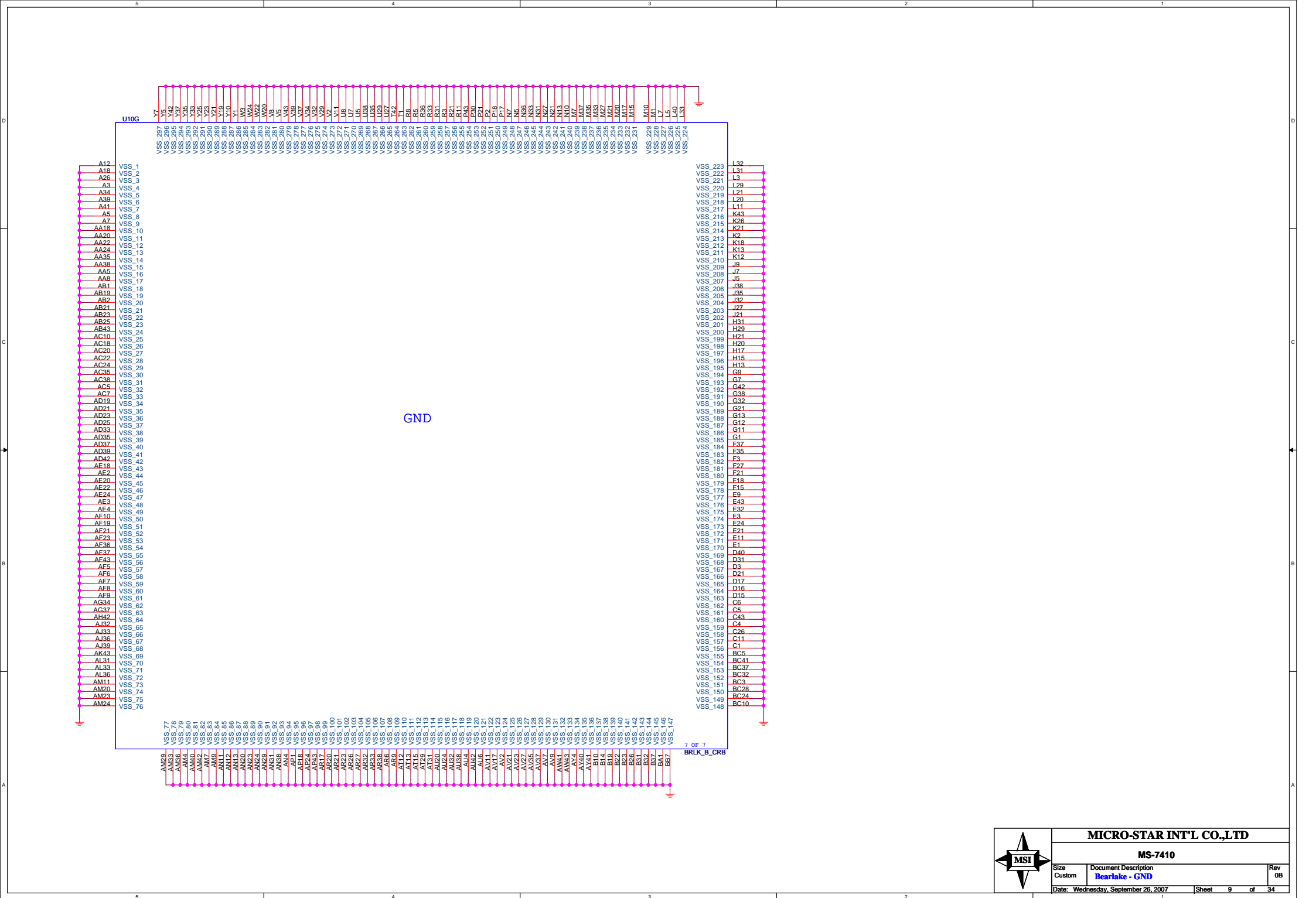


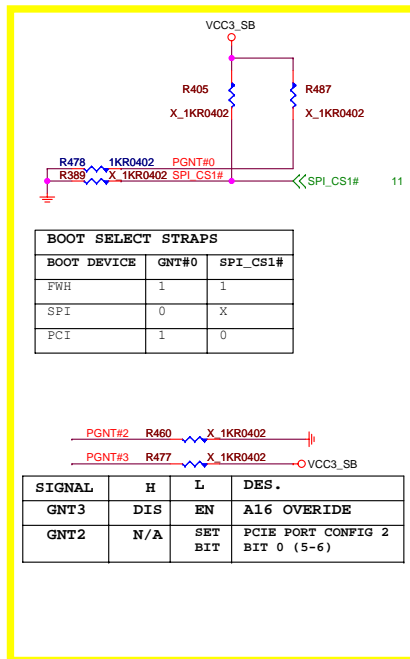
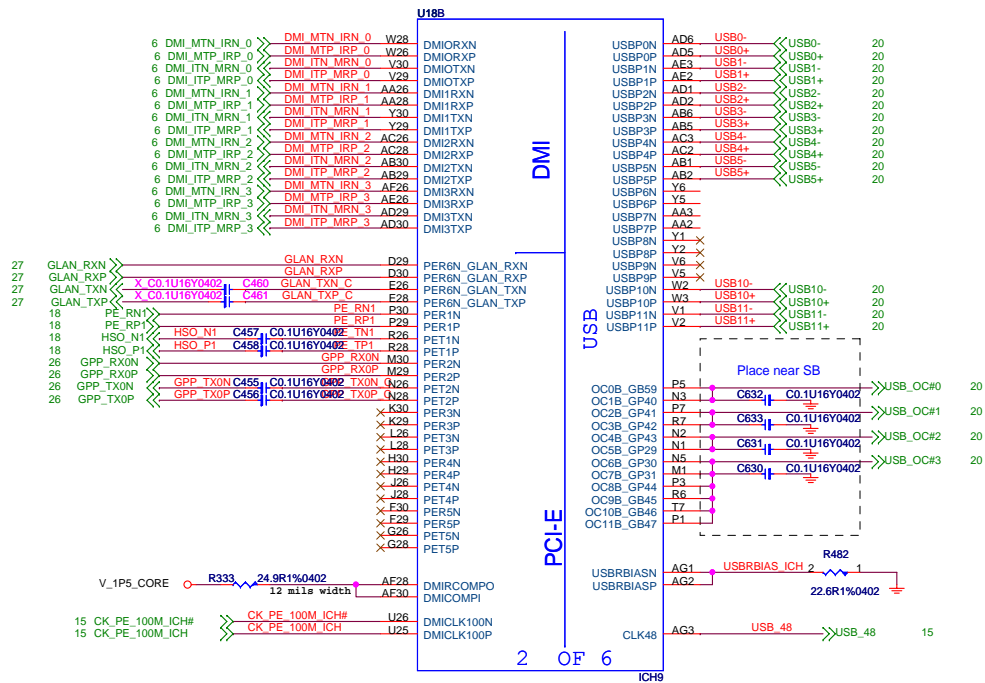
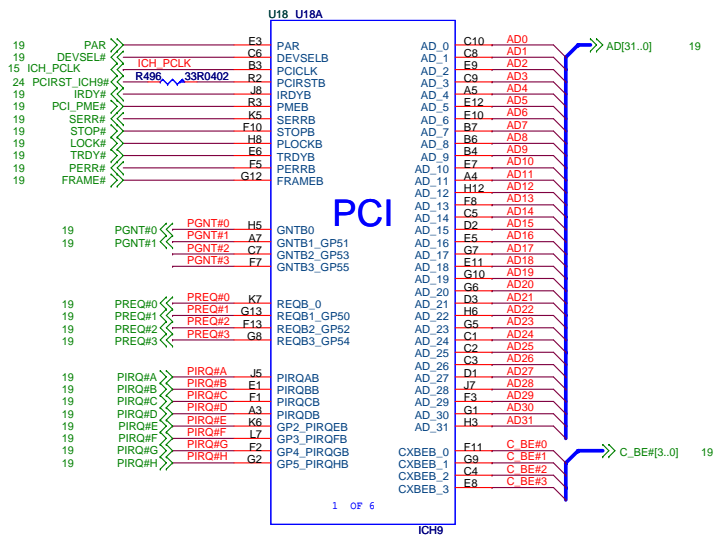




MICRO-STAR INT'L CO.,LTD		
MS-7410		
Size	Document Description	Rev
Custom	Bearlake - Memory	08
Date: Wednesday, September 26, 2007		
Sheet 7 of 34		



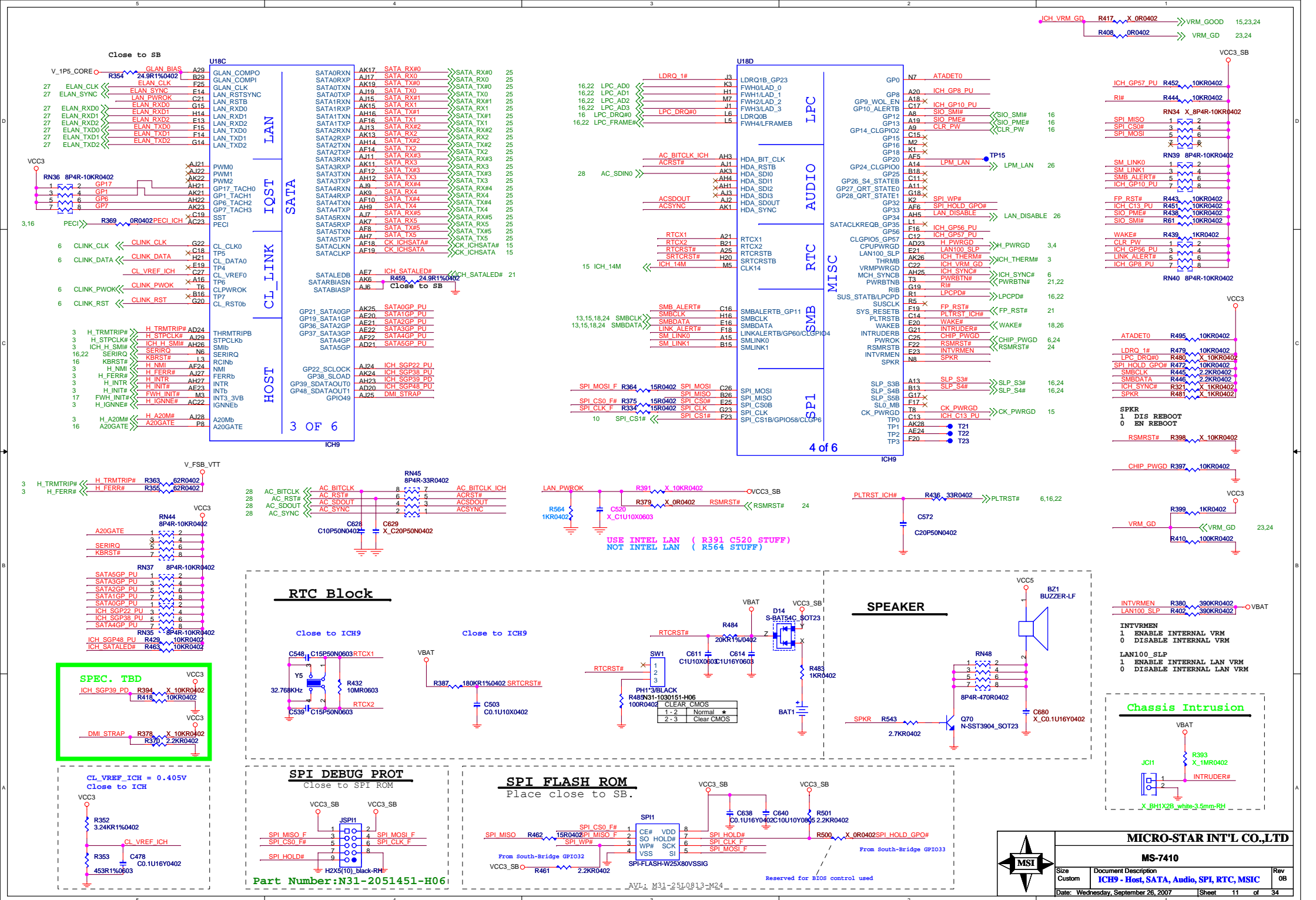




ICH9 H/W STRAPS			
SIGNAL	H	L	DES.
SPKR	DIS	EN	REBOOT
GNT3	DIS	EN	A16 OVERRIDE
INTVRMEN	EN	DIS	INT VRM
SATALED	NORM	REVERSE	PCIE 0-3 ORDER
HDA_SDOUT	DFX/PCIE	N/A	XOR MODE/PCIE PORT CONFIG BIT 1
HDA_SYNC	SET BIT	N/A	PCIE PORT CONFIG BIT 0 (1-4)
GNT2	N/A	SET BIT	PCIE PORT CONFIG 2 BIT 0 (5-6)

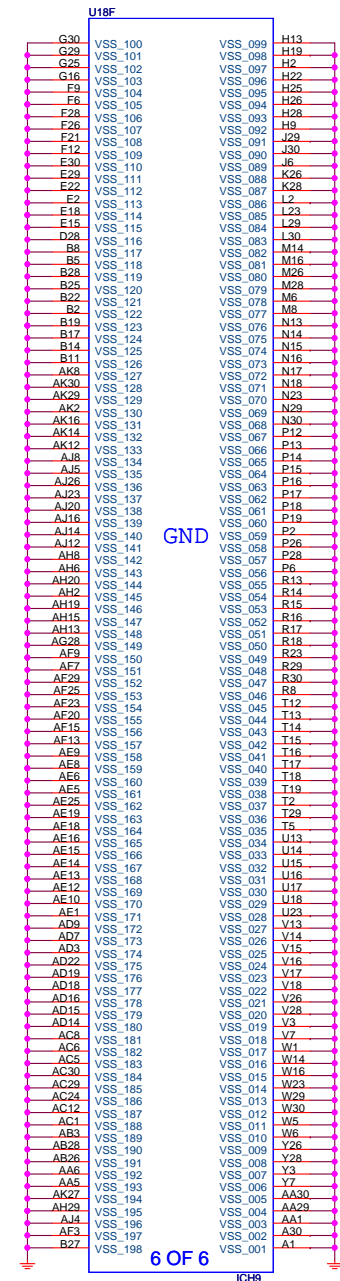
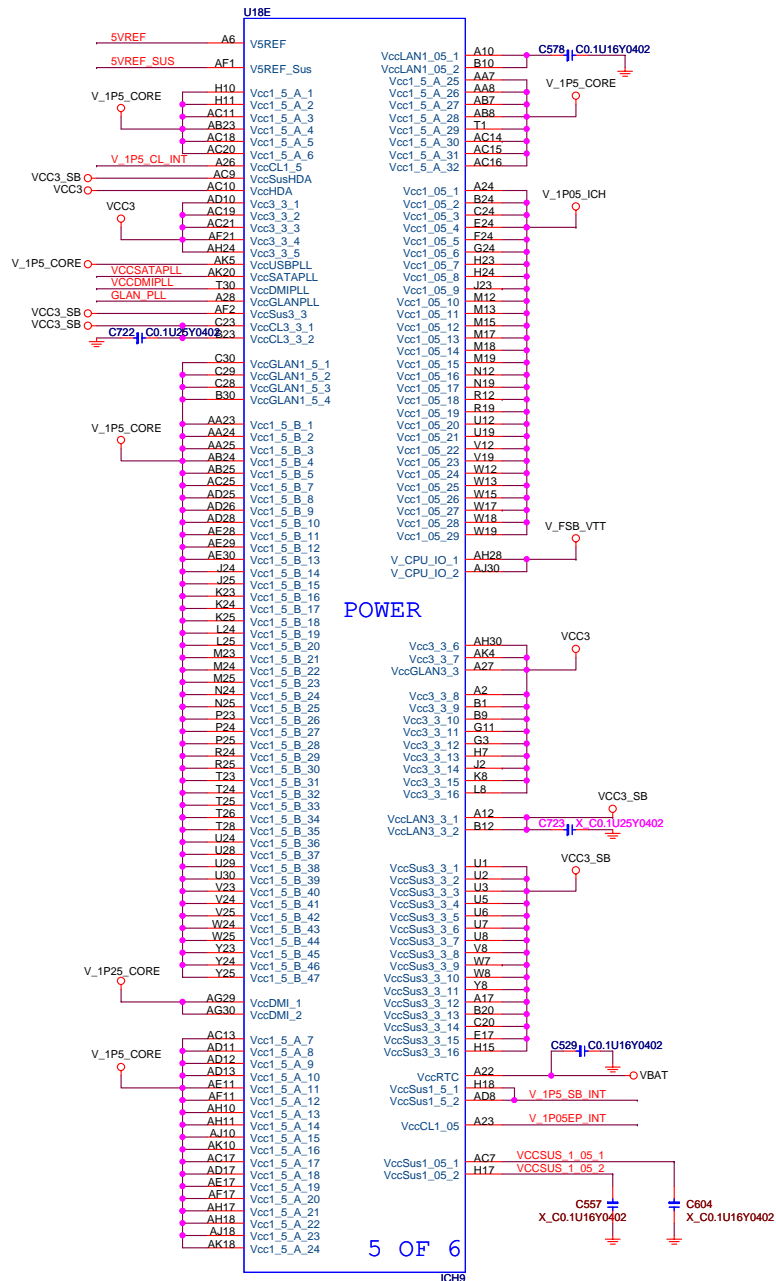
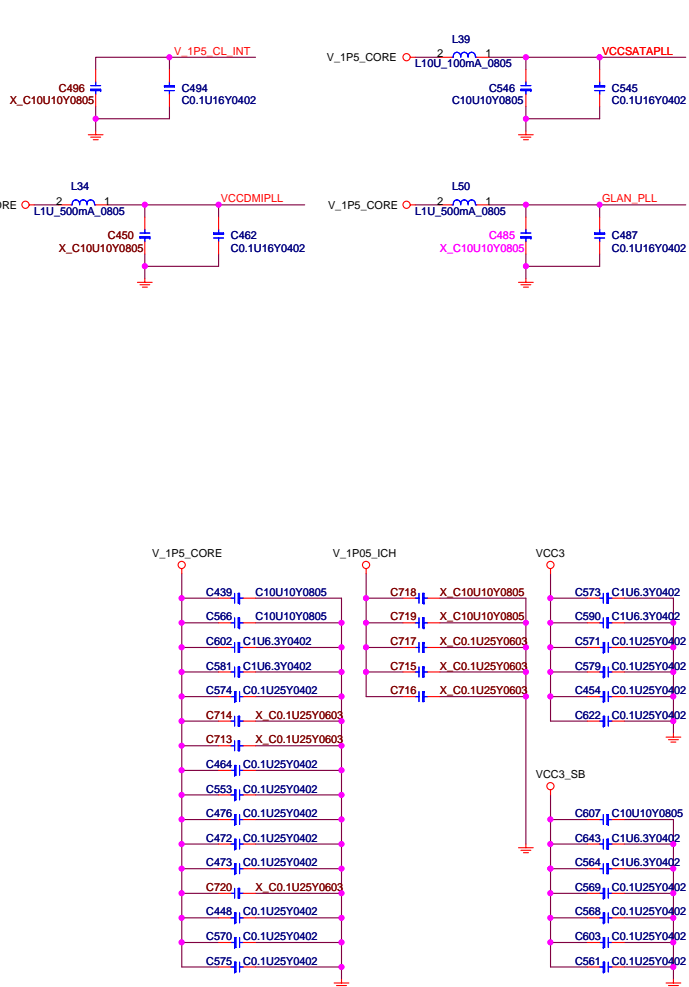
BOOT SELECT STRAPS		
BOOT DEVICE	GNT#0	SPI_CS1#
FWH	1	1
SPI	0	X
PCI	1	0

SIGNAL	H	L	DES.
GNT3	DIS	EN	A16 OVERRIDE
GNT2	N/A	SET BIT	PCIE PORT CONFIG 2 BIT 0 (5-6)



5VREF & 5VREF_SUS Sequencing Circuit

The diagram illustrates the sequencing circuit for 5VREF and 5VREF_SUS. It consists of two identical PMOS transistor-based switches (Q59 and Q61) controlled by VCC3 and VCC3_SB. The gates of Q59 and Q61 are connected to VCC3 and VCC3_SB, respectively. The sources are connected to VCC5 and VCC5_SB. The drains are connected to a 10R0402 resistor, which is then connected to a 10R0402 resistor leading to the 5VREF and 5VREF_SUS pins. A capacitor C580 (C0.1U16Y0402) is connected between the 5VREF pin and ground, and a capacitor C612 (C0.1U16Y0402) is connected between the 5VREF_SUS pin and ground.



MICRO-STAR INT'L CO.,LTD

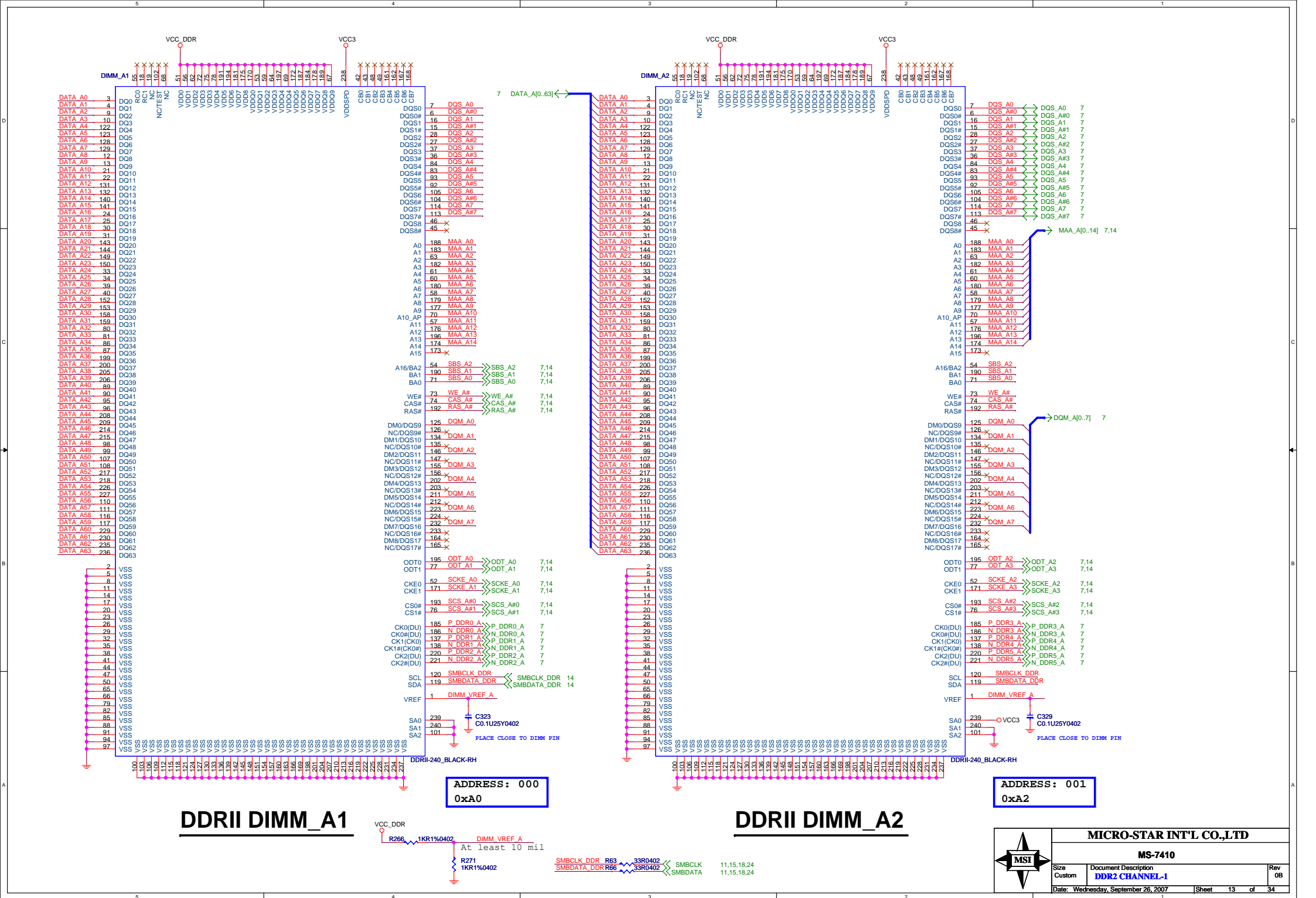
MS-7410

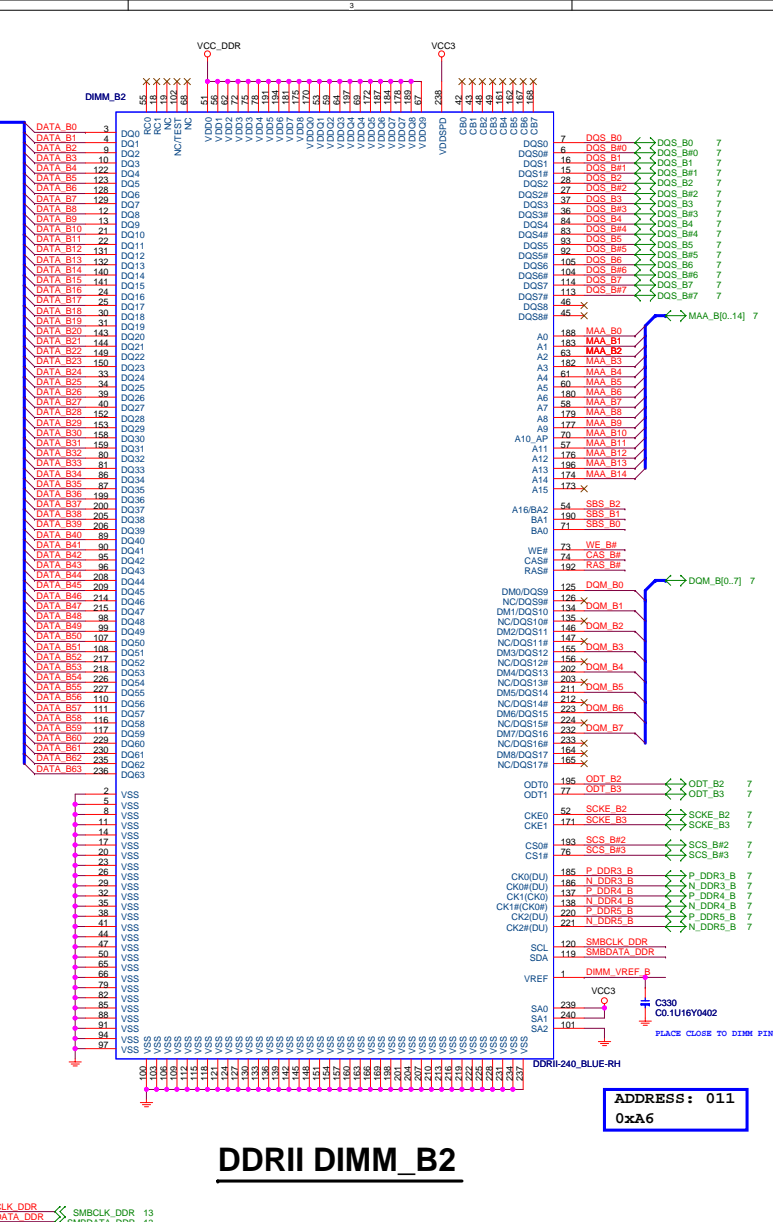
Size	Custom
------	--------

Document Description
ICH9 - Power, GND

Rev	0B
-----	----

Date: Wednesday, September 26, 2007 Sheet 12 of 34





MS-7410		
Size Custom	Document Description DDR2 CHANNEL-2/DDR II Termination	Rev 01
Date: Wednesday, September 26, 2007		Sheet 14 of 34

VCC3

1.2μF

FB0R3AD07R5R

C428 Co.1U16Y0402

CKVDD

C526 C471 0X0805

C466 Co.1U16Y0402

C507 Co.1U16Y0402

C437 Co.1U16Y0402

C488 Co.1U16Y0402

C525 Co.1U16Y0402

CKVDD_IO

1.2μF

0R0805

C431 Co.1U16Y0402

C426 C10U10Y0805

C428 C10U10Y0805

C430 C10U10Y0805

C427 Co.1U16Y0402

C422 Co.1U16Y0402

C432 Co.1U16Y0402

C483 Co.1U16Y0402

VDD_IO

PC1_CLK1 C510 X C10P50N0402

PC1_CLK2 C498 X C10P50N0402

PC1_CLK0 C524 X C10P50N0402

ICH_PCLK C483 X C10P50N0402

SIO_PCLK C541 X C10P50N0402

USB_48 C475 X C10P50N0402

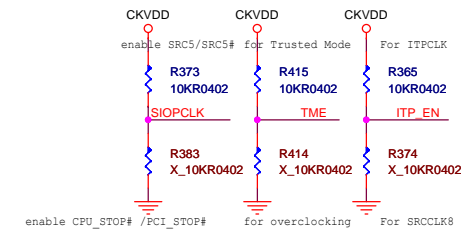
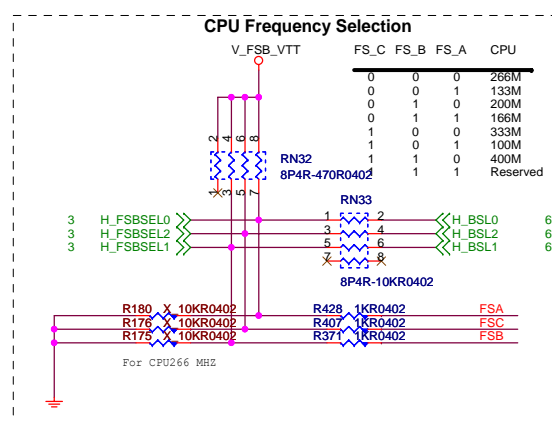
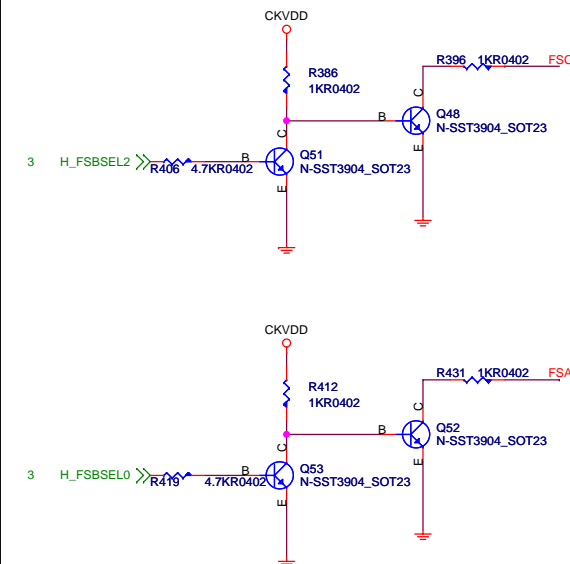
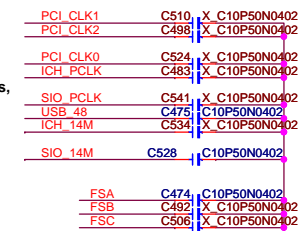
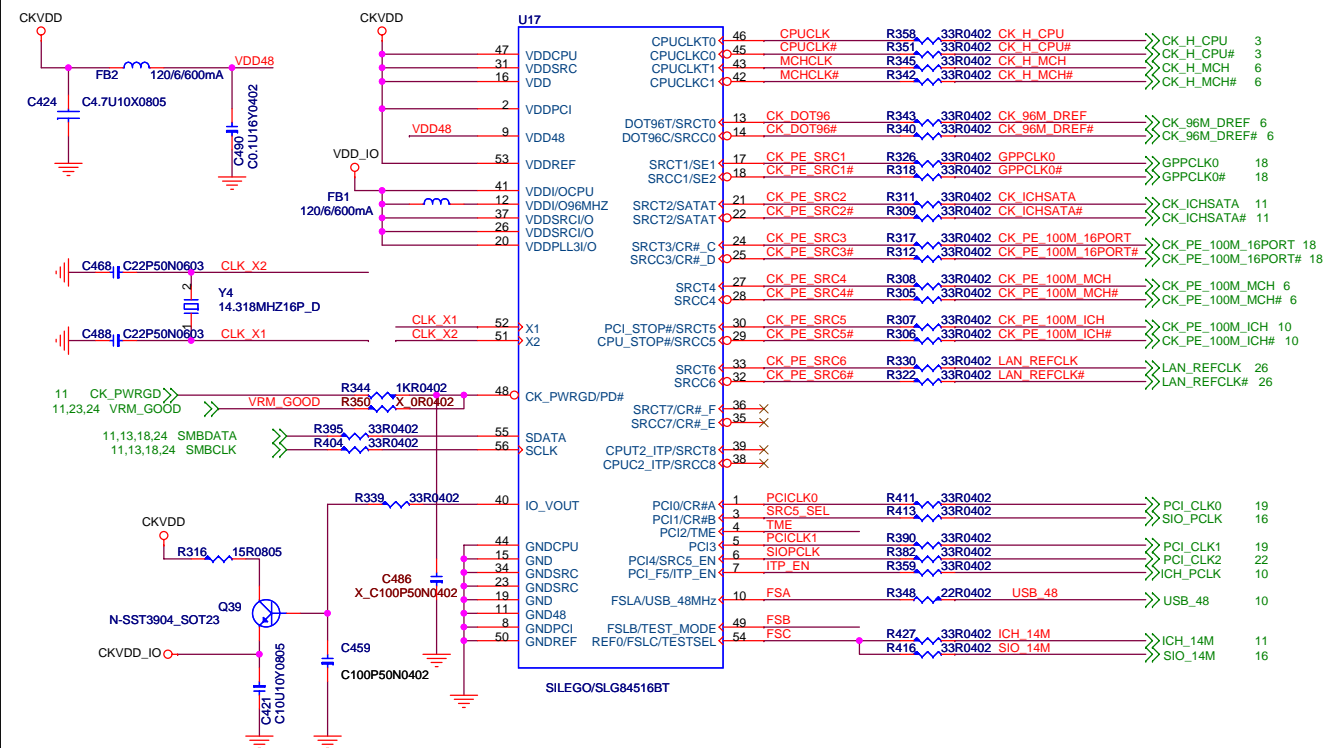
ICH_14M C534 X C10P50N0402

SIO_14M C528 C10P50N0402

FSA C474 C10P50N0402

FSB C492 X C10P50N0402

FSC C506 X C10P50N0402



MICRO-STAR INT'L CO.,LTD

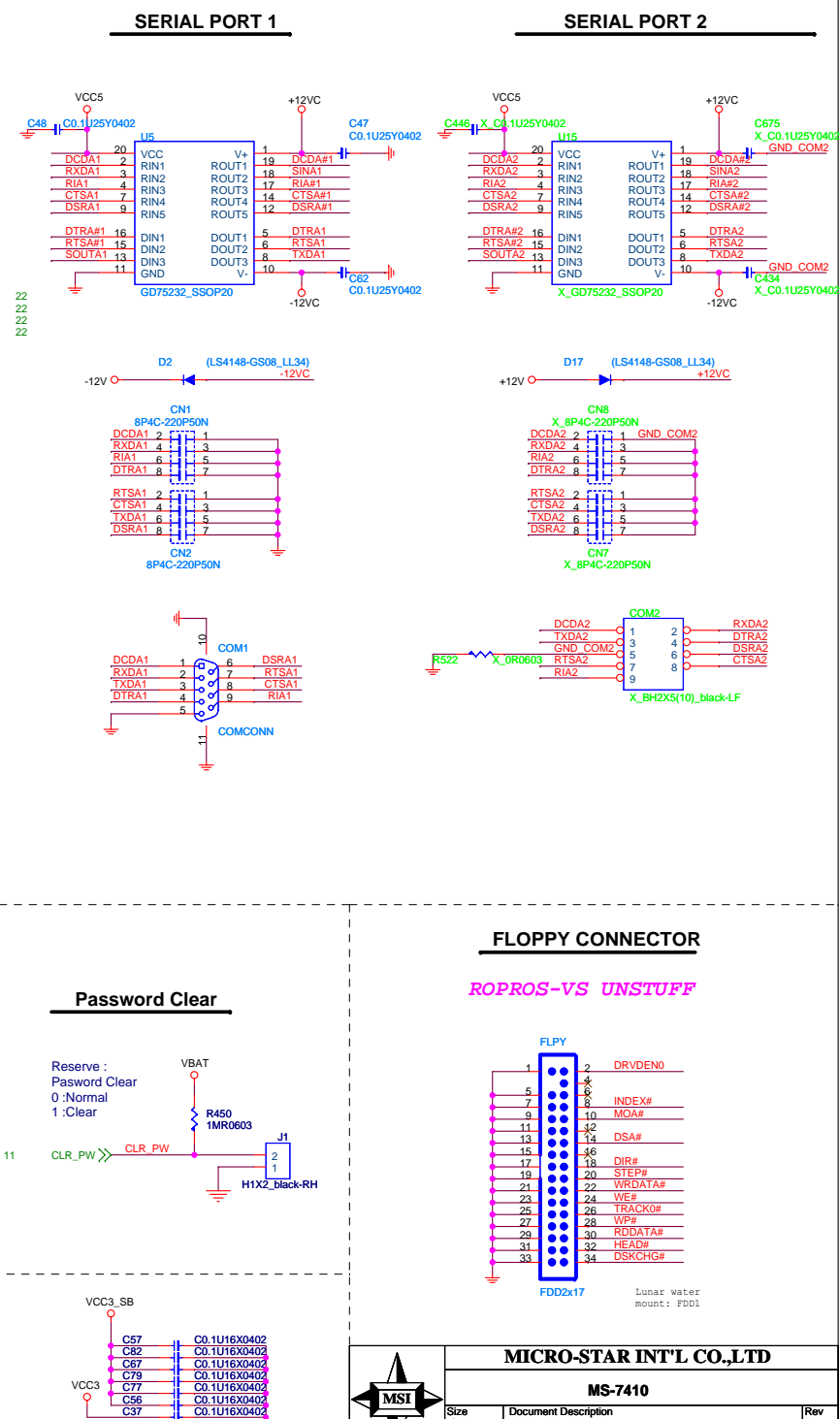
MS-7410

Size Custom	Document Description SLG84516BT CLK Gen.
----------------	--

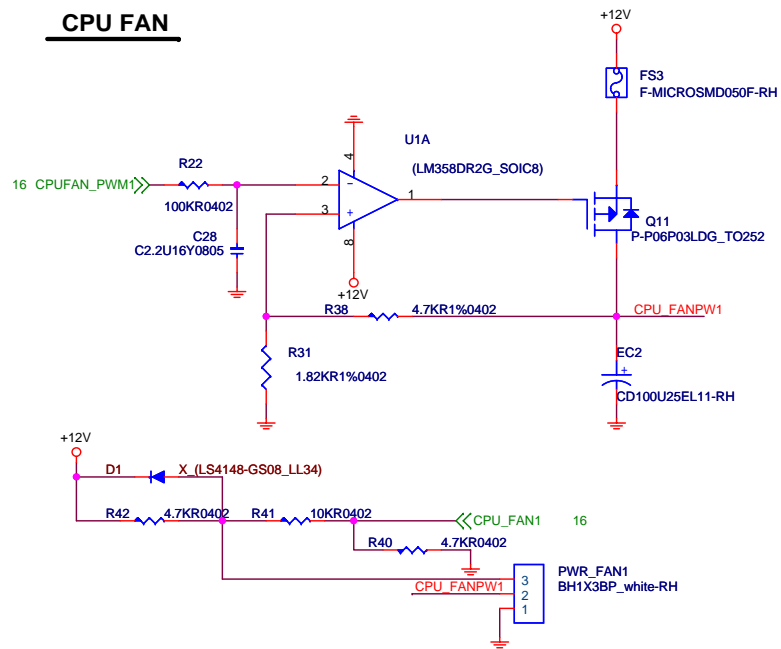
Date: Wednesday, September 26, 2007

Rev	0B
-----	----

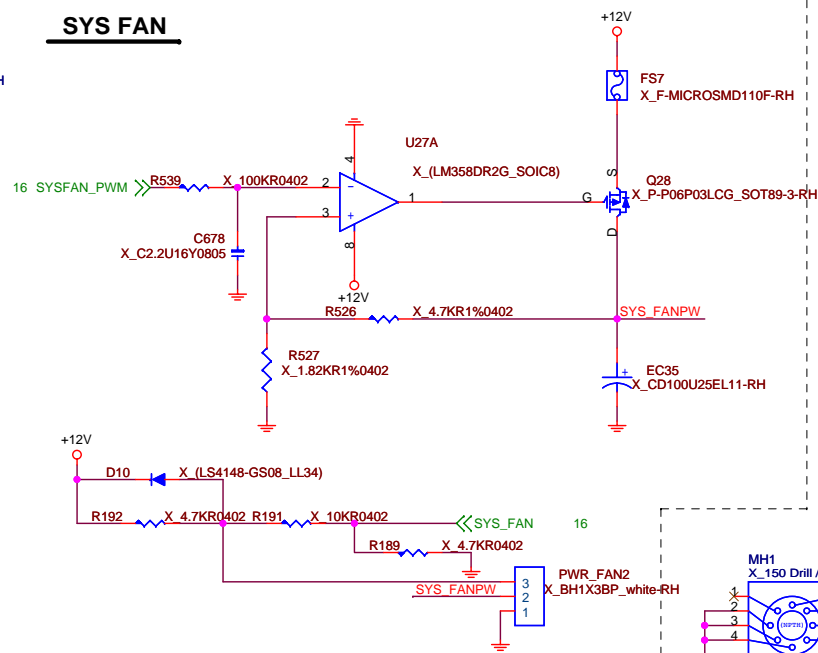
of 3



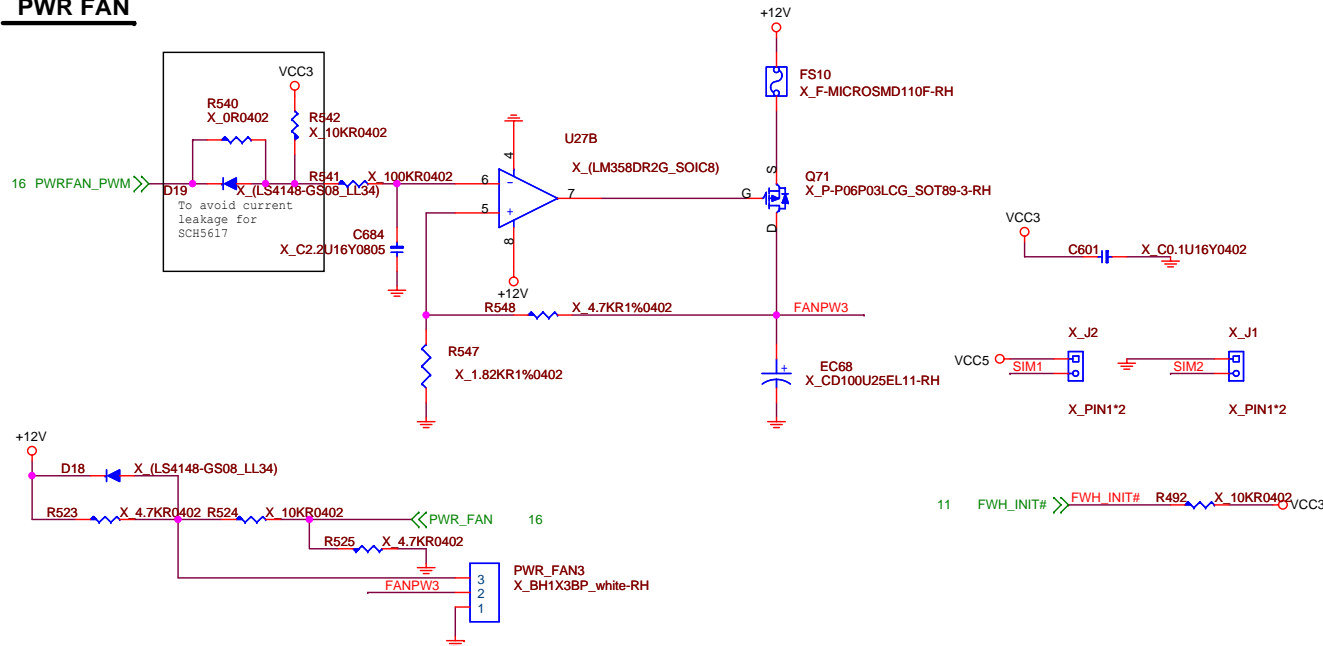
CPU FAN



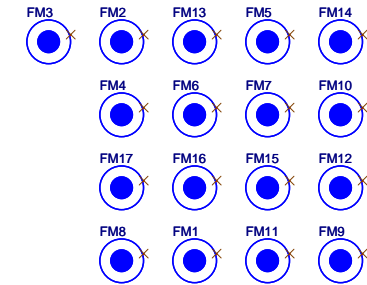
SYS FAN



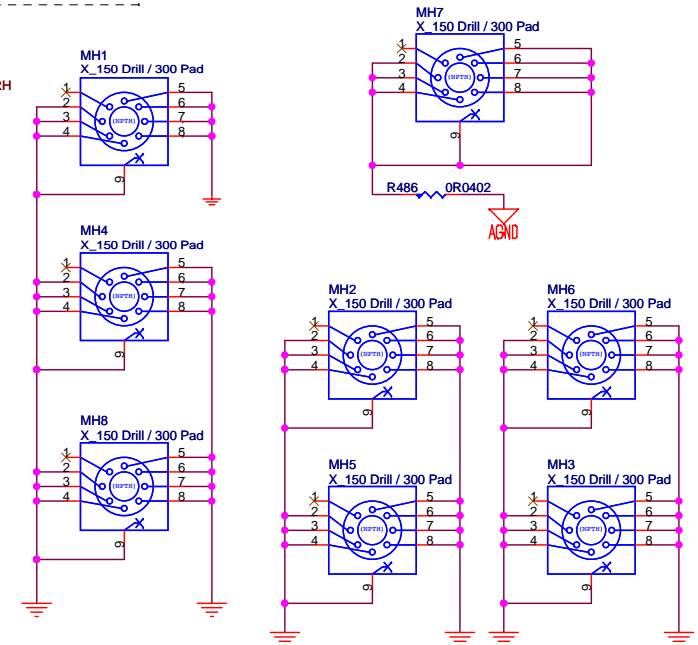
PWR FAN




Optical Fiducial Marks

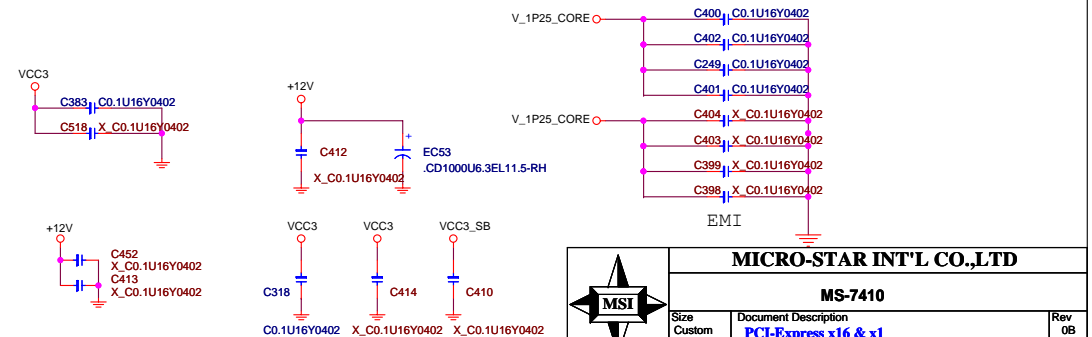
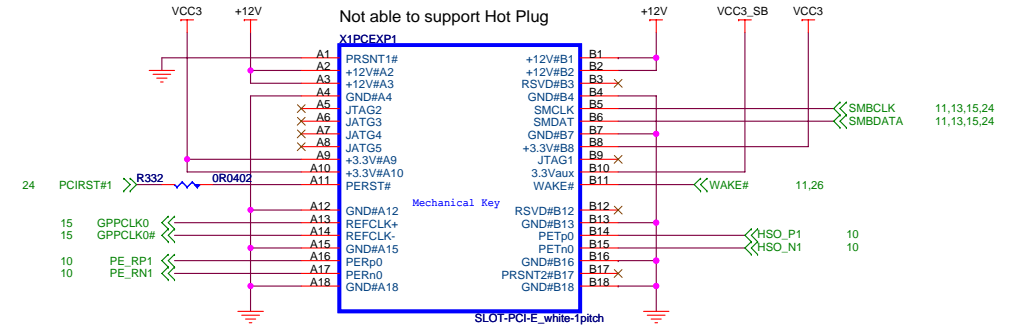
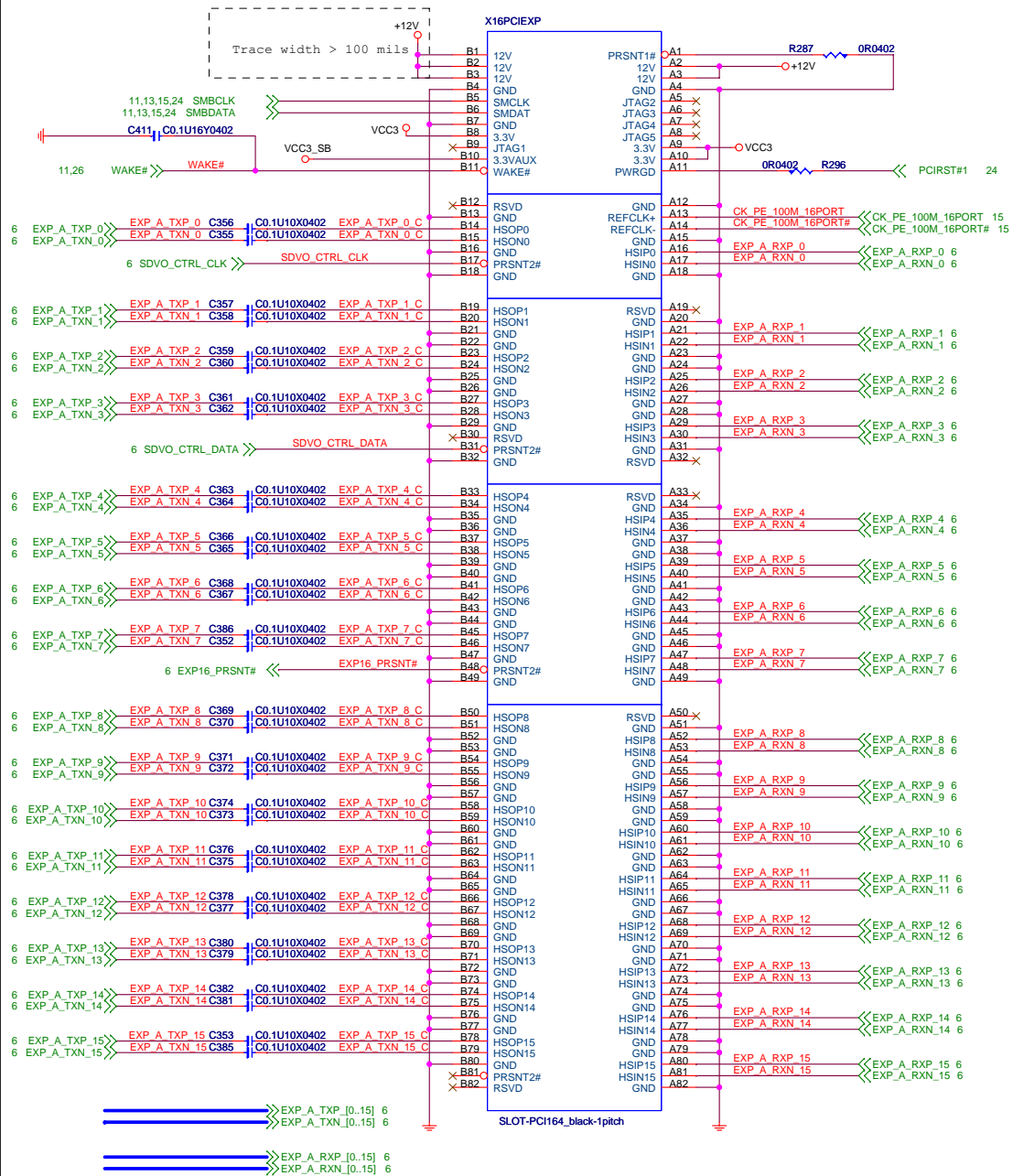


Mounting Holes

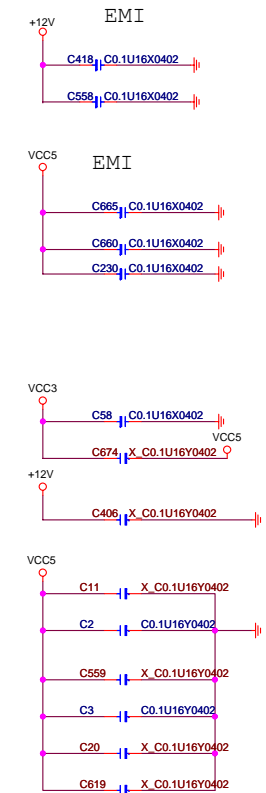
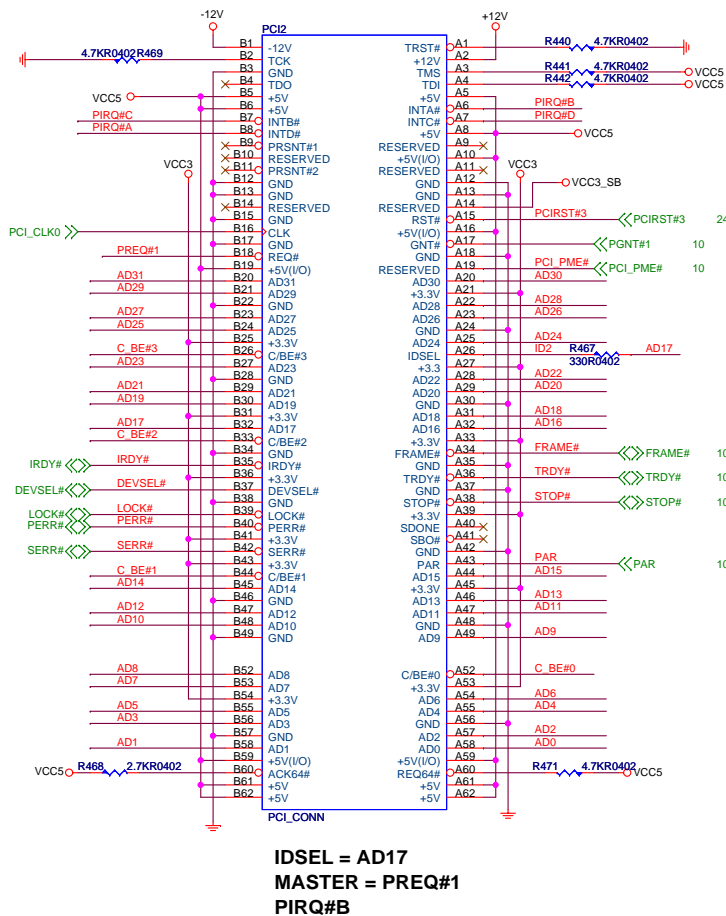


			
MICRO-STAR INT'L CO.,LTD			
MS-7410			
Size B	Document Description		Rev 0B
	CPU/SYS/PWR FAN		
Date: Wednesday, September 26, 2007		Sheet 17	of 34

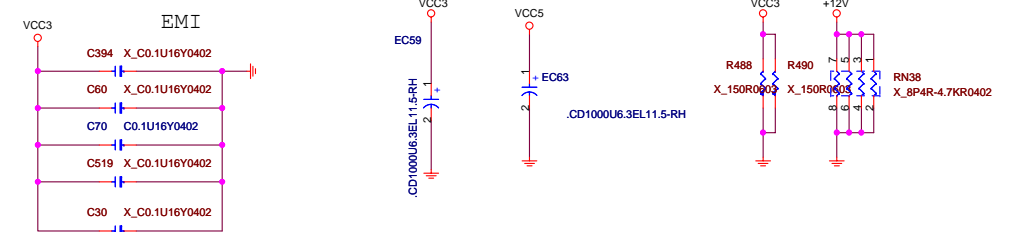
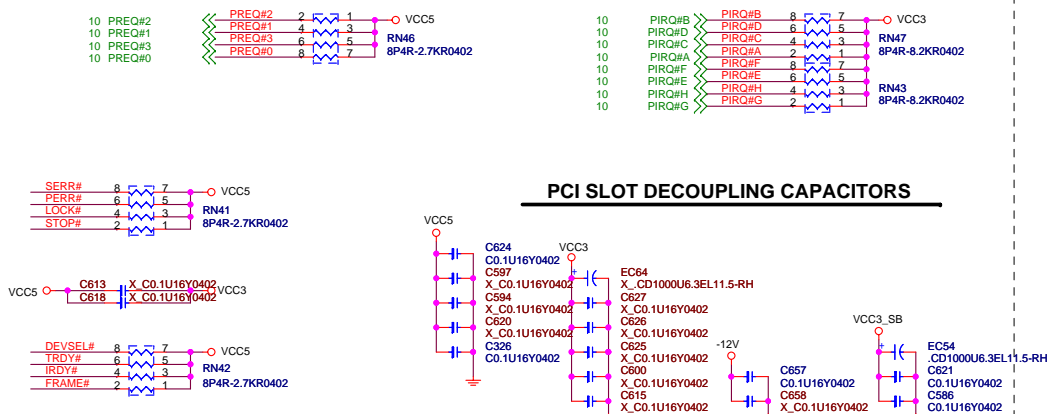
PCI EXPRESS 16-PORT



PCI SLOT 2 (PCI VER: 2.2 COMPLY)



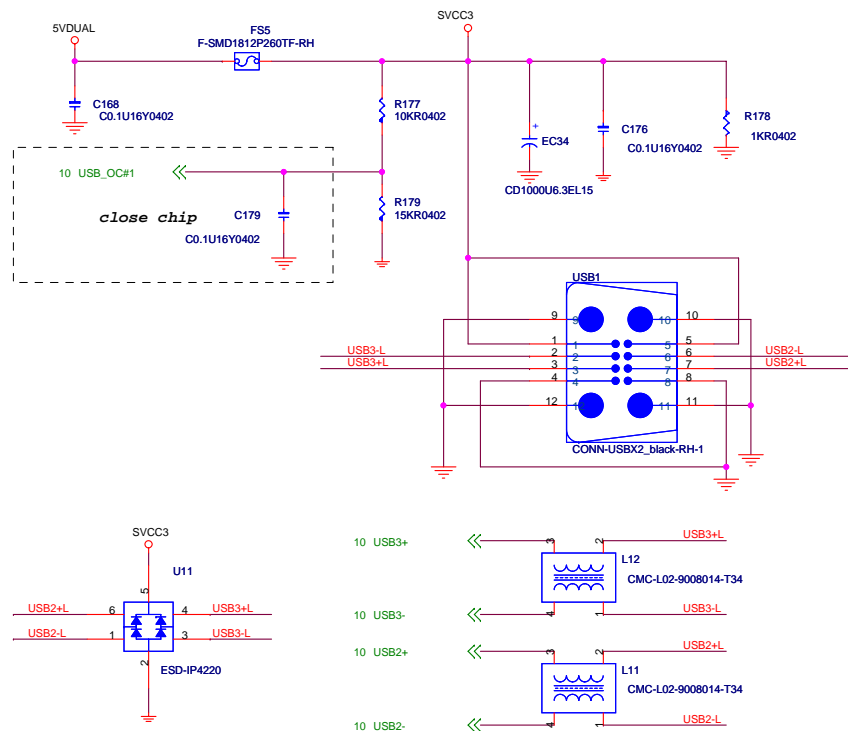
PCI SLOT DECOUPLING CAPACITORS



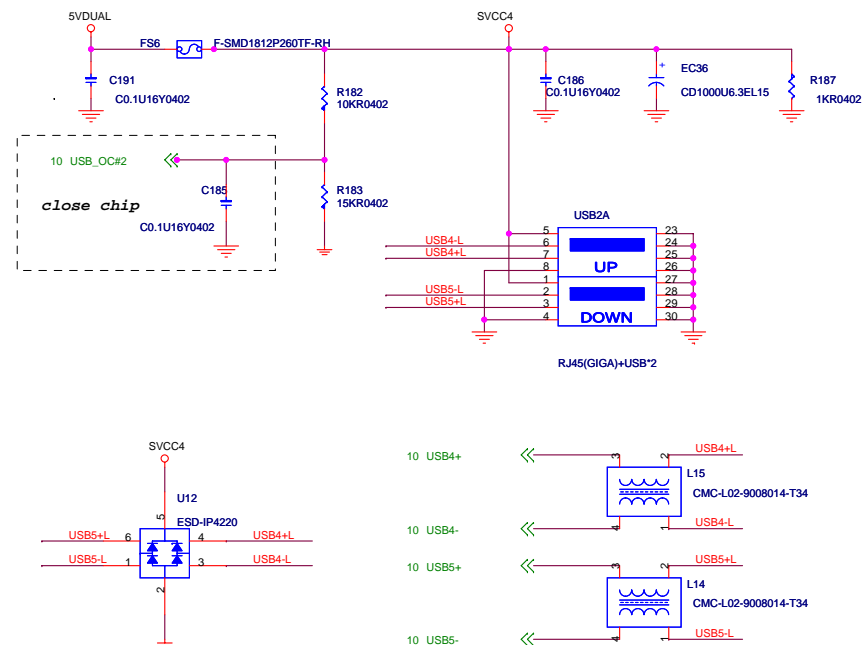
MS-7410

Size Custom	Document Description PCI Slot	Rev 0B
Date: Wednesday, September 26, 2007	Sheet 19 of 34	

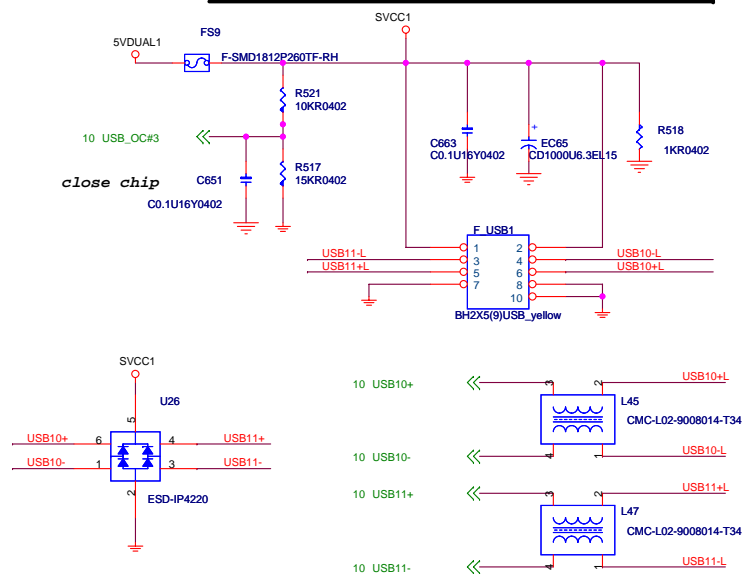
REAR PANEL USB CONNECTOR FOR USB PORT 2,3



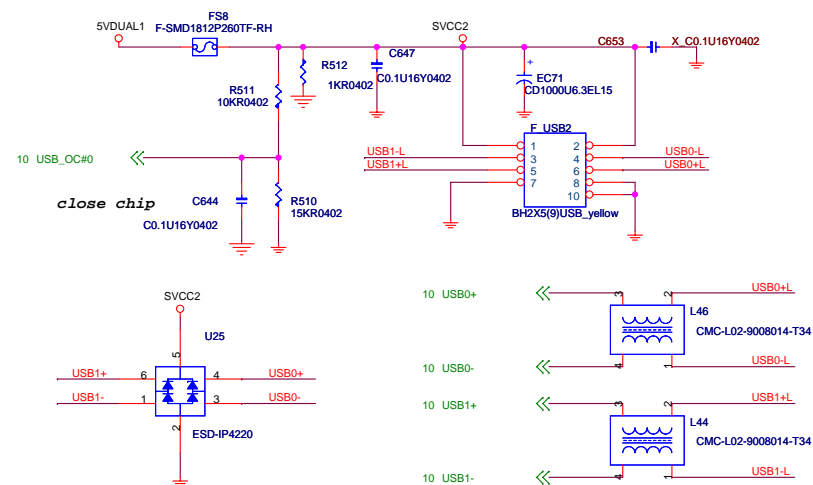
REAR PANEL USB CONNECTOR FOR USB PORT 4,5



Front USB PORT 10,11 (right angel type)



Memory card reader USB CONNECTOR FOR USB PORT 0,1

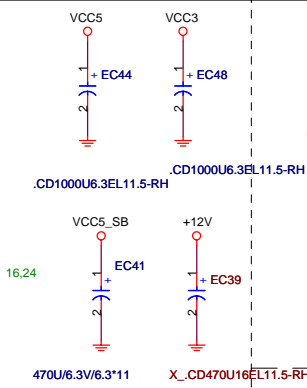
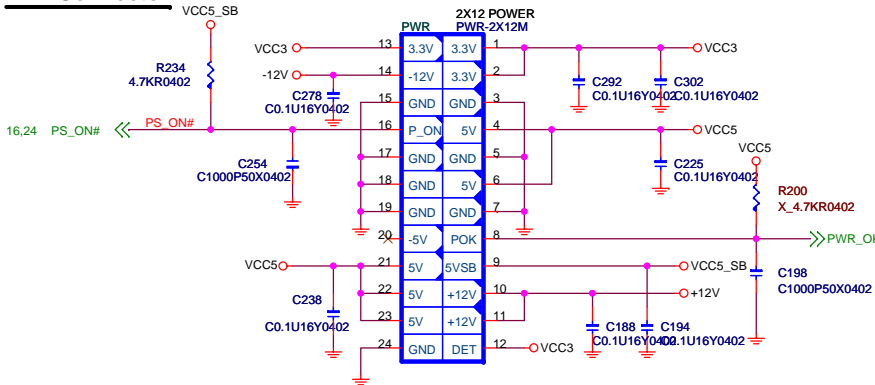


MICRO-STAR INT'L CO.,LTD

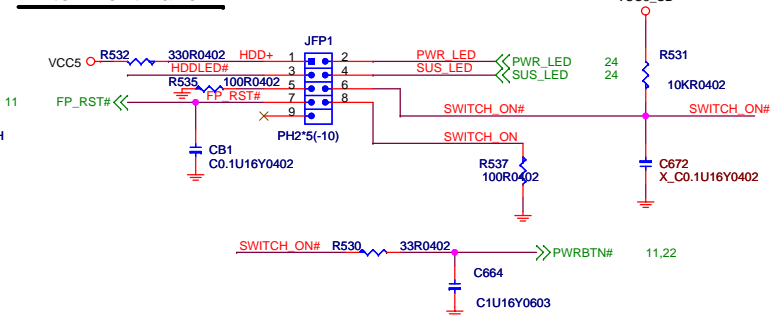
MS-7410

Size	Document Description	Rev
Custom	USB CONNECTORS	0B
Date: Wednesday, September 26, 2007	Sheet 20 of 34	

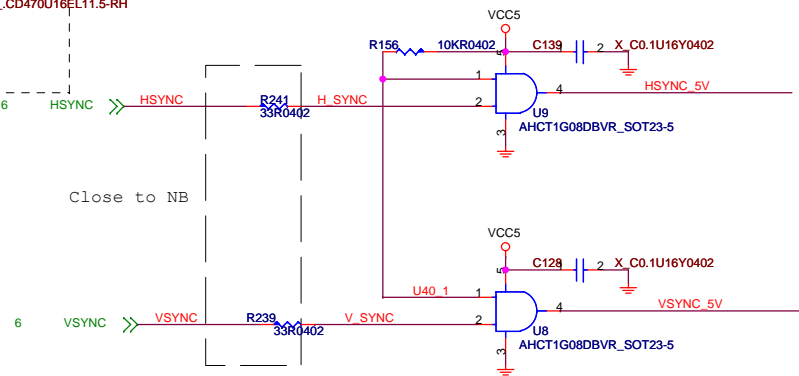
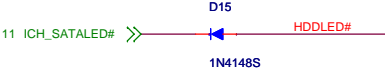
ATX Connector



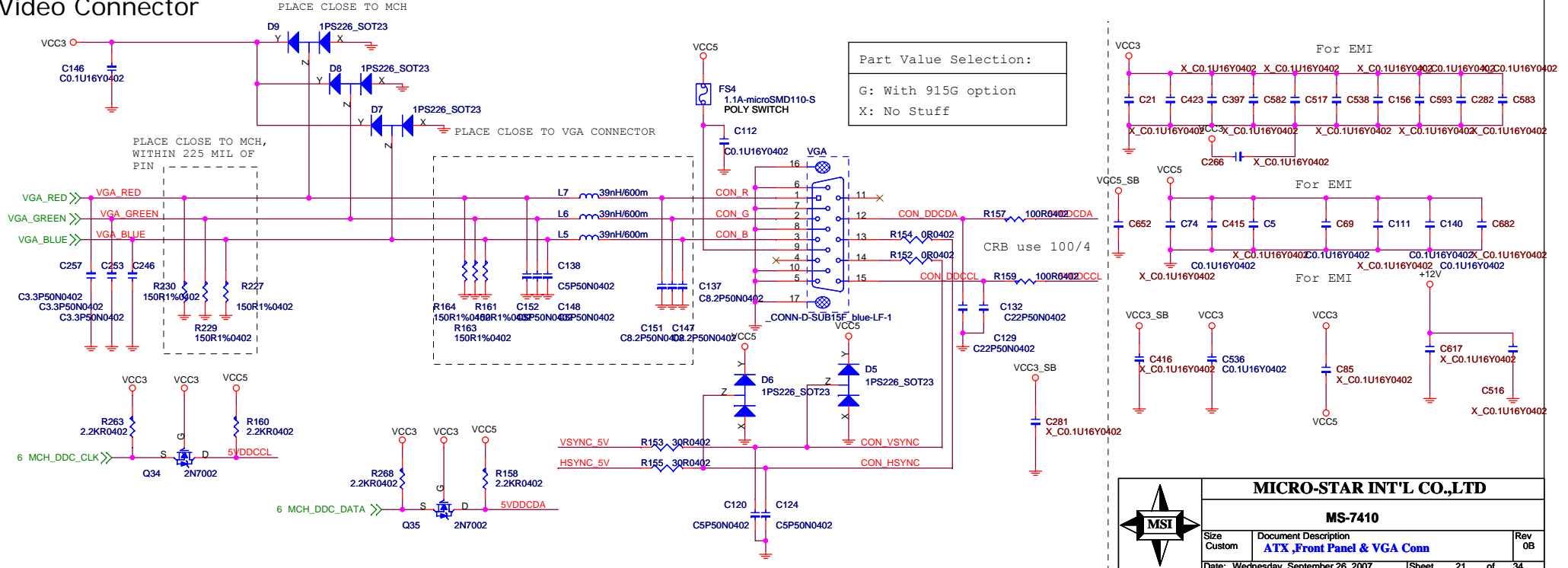
Intel Front Panel



IDE LED



Video Connector



MICRO-STAR INT'L CO.,LTD

MS-7410

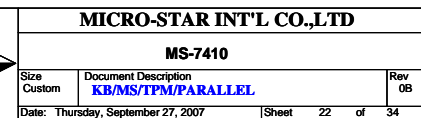
Size Custom

Document Description
ATX,Front Panel & VGA Conn

Rev
0B

Date: Wednesday, September 26, 2007

Sheet 21 of 34

[illegible][illegible]

Voltage Regular Module

N-P0903BDG_TO252
P75N02LDG/TO252
C100U2SP
CD560U40S-2
1800UF/6.3V
0.25uH/40A
CH-1.1U25A-LF
CD1000U16EL20-2

mosfet/n-channel, P0903BDG, SMT/TO252, Rds(on)=9.5mΩ(10V, 25A), Vgs(on)=1~3V, Id=50A, Ciss=1800pF, Qg=50nC, Vds=25V, Vgs=±20V, RoHS compliance

mosfet/n-channel, P75N02LDG, SMT/TO252, Rds(on)=7mΩ(10V, 30A), Vgs(on)=1~3V, Id=75A, Ciss=5000pF, Qg=140nC, Vds=25V, Vgs=±20V, RoHS compliance

ESR<13mΩ, Ripple cur.<2.7A, 13mΩ, 105C

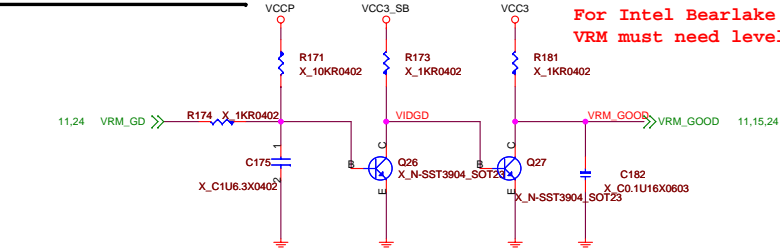
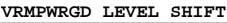
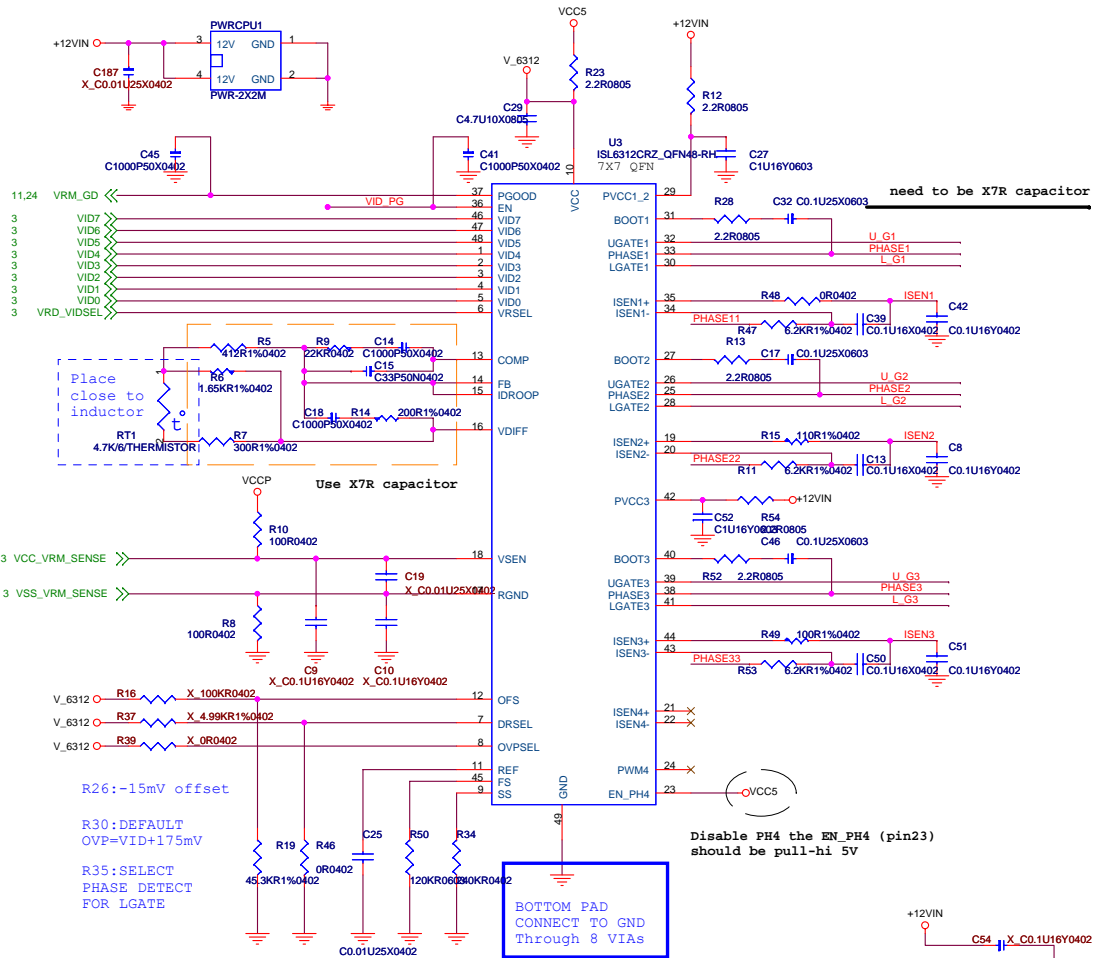
CAP, OS-CON, 560u/4V, Dip-2/8*9/3.5mm, ESR<7mohm, Ripplecur.=6100mA, Lc. <500uA, SPEC series, RoHS compliance

ESR<12mΩ, Ripplecur<2350mA, 105C, longlife change from 2000hrs to 3000hrs, KZJ series

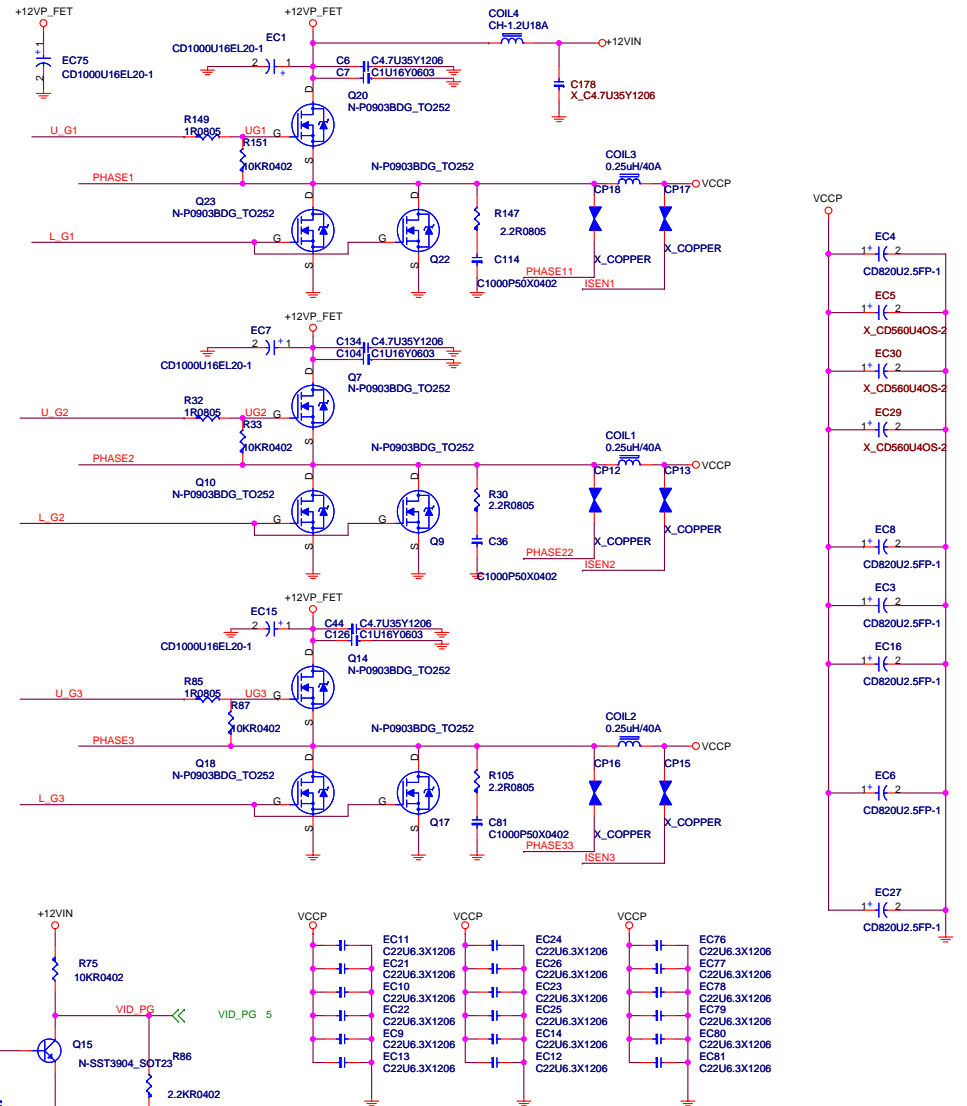
, IND CHOKE, 0.25uH, 20%, DIP/8.5mm, 40A, 0.6mOhm, , , PEW, FERRITE, SQUARE, RoHS COMPLIANCE

IND CHOKE, 1.1uH, 20%, DIP/9mm, 25A, 1.4mOhm, 5.5T, 0.9mmx3, PEW, IRON, , LEAD FREE

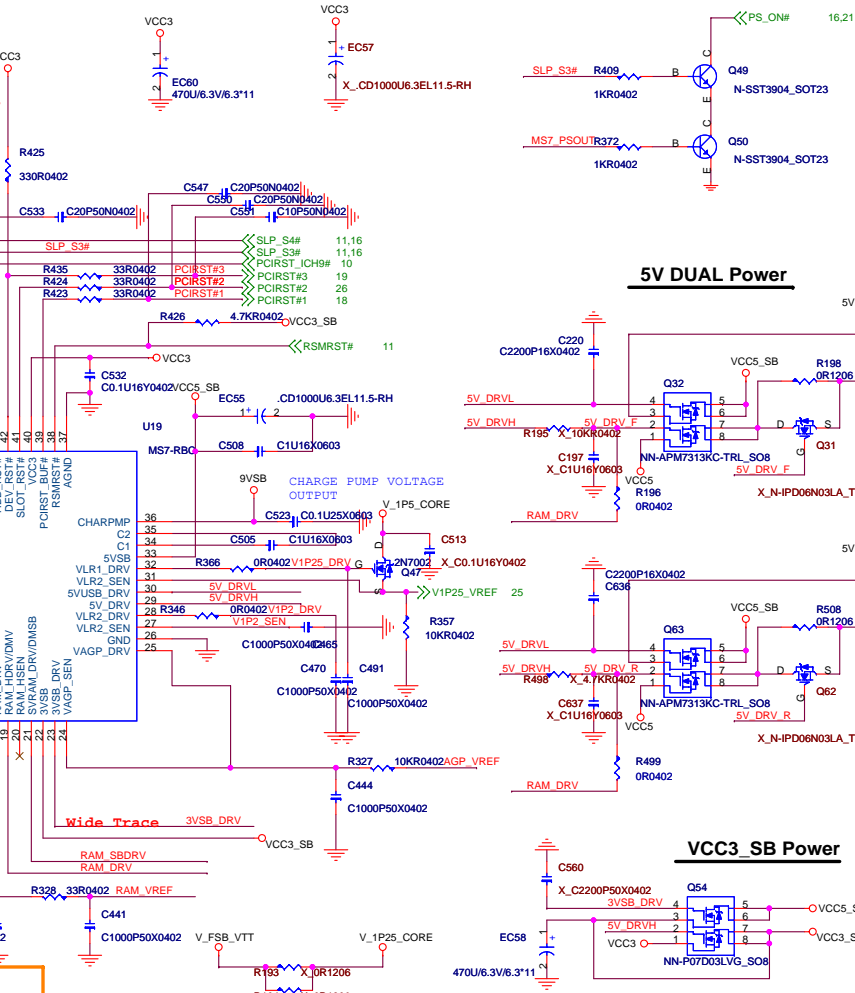
CAP, EL, 1000u, 16V, Dip-8x20/3.5mm, 20%, 12mOhm, 2350mA, 105C, 3000hrs, RoHS COMPLIANCE



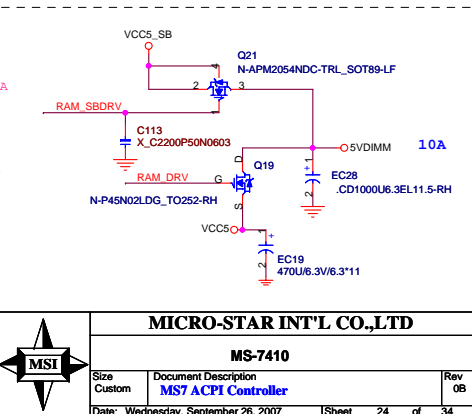
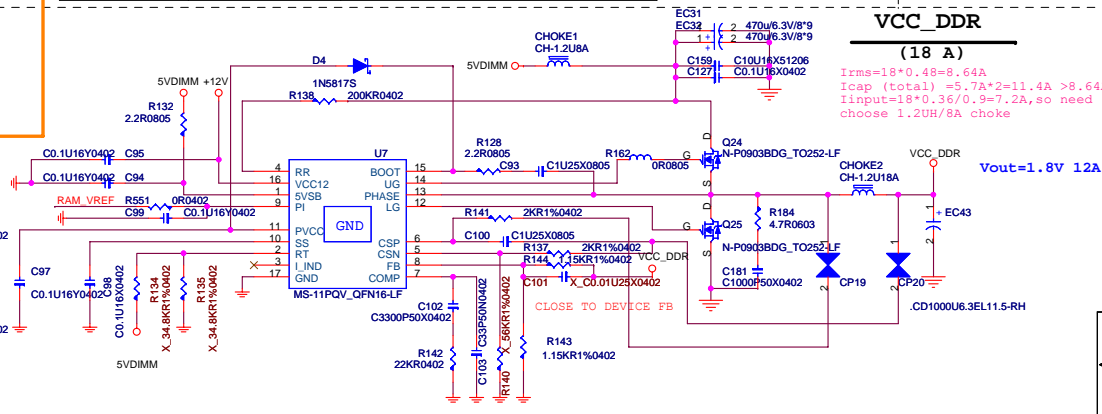
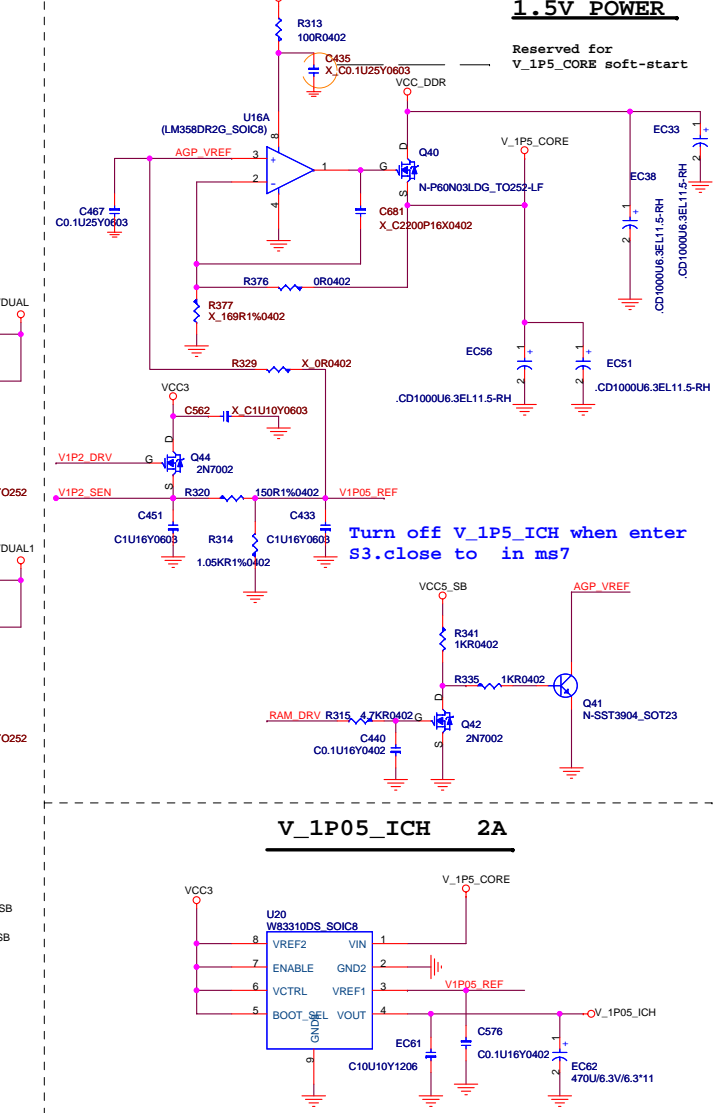
For Intel Bearlake Design Guide.
VRM must need level shift



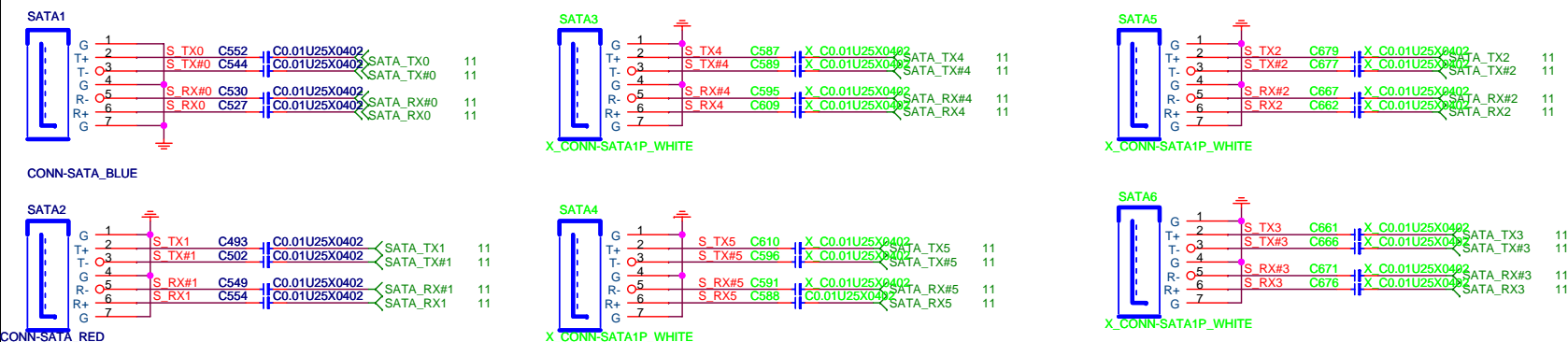
MICRO-STAR INT'L CO.,LTD			
MS-7410			
Size Custom	Document Description VRD11 Intersil 6312 3Phase		Rev 0B
Date: Thursday, September 27, 2007		Sheet 23 of 34	



VTT_SEL = L	V_FSB_VTT=1.1V	For future KENTSFIELD processor. (FSB1333, Quad-Core)
VTT_SEL = H	V_FSB_VTT=1.2V	For normal processors.

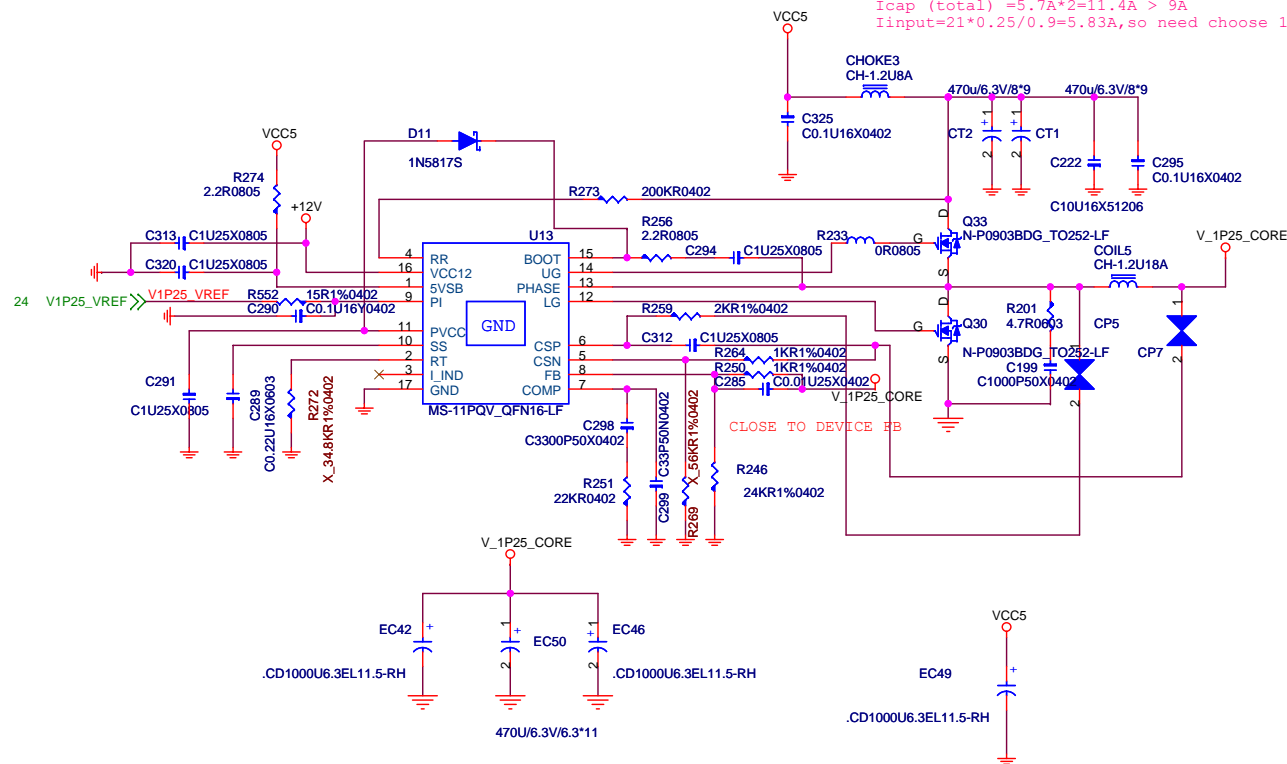


SERIAL ATA CONNECTOR BLOCK **SATA1&SATA2 FOR ROPROS-MA/VS USE**



GMCH 1.25V POWER
(21.3A)

$I_{rms} = 21 \times 0.433 = 9.09A$
 $I_{cap} \text{ (total)} = 5.7A \times 2 = 11.4A > 9A$
 $I_{input} = 21 \times 0.25 / 0.9 = 5.83A$, so need choose 1.2UH/8A choke



MICRO-STAR INT'L CO.,LTD

MS-7410Size
B

Document Description
SATA&V 1P25 CORE

Rev	0B
-----	----

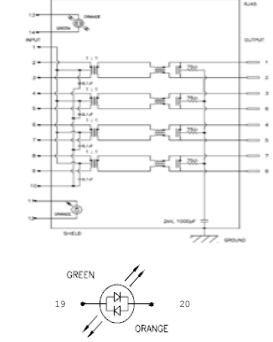
Date: Wednesday, September 26, 2007

Sheet 25 of 34

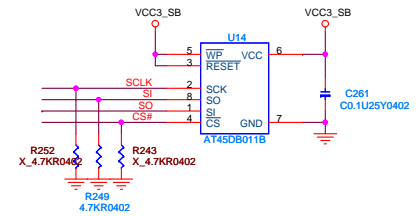
BCM5787M LAN CHIP (ROPROS-MA/NECCAP USE)

LAN Connector

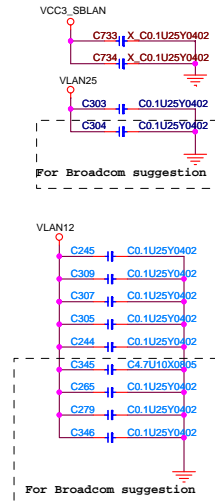
Giga-Lan	
N58-22F0271-S42	
Link	Yellow
Active	Blinking
1000	Orange
100	Green
10	None
21	Orange
22	Yellow
20	Orange
19	Green



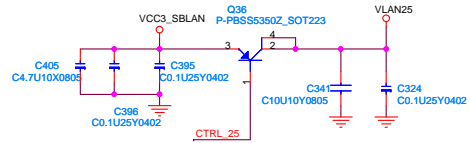
LAN EEPROM



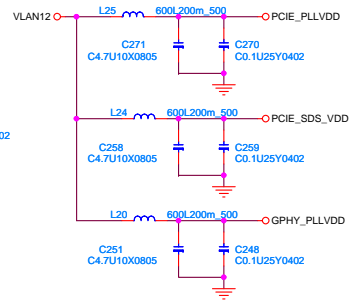
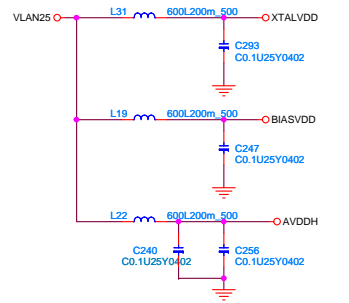
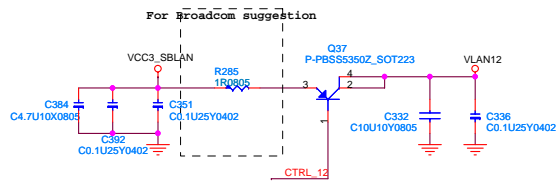
Bypass CAPs



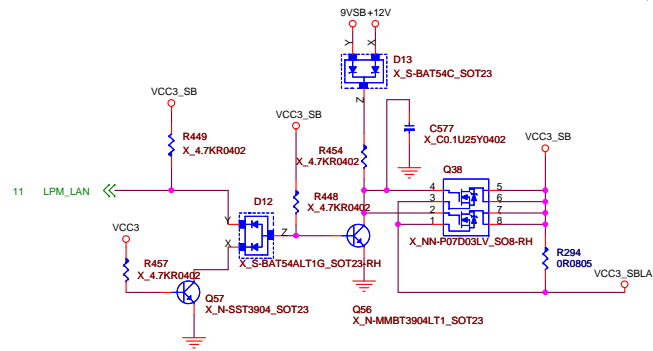
LAN 2.5 POWER (235mA)



LAN 1.2 POWER (590mA)

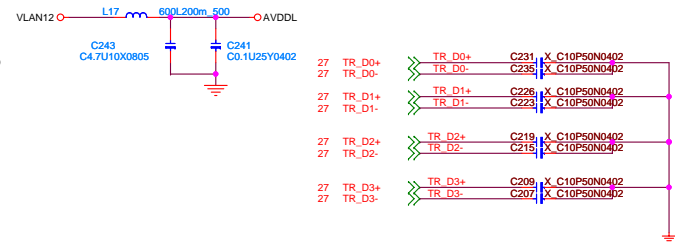


Power control for power consumption

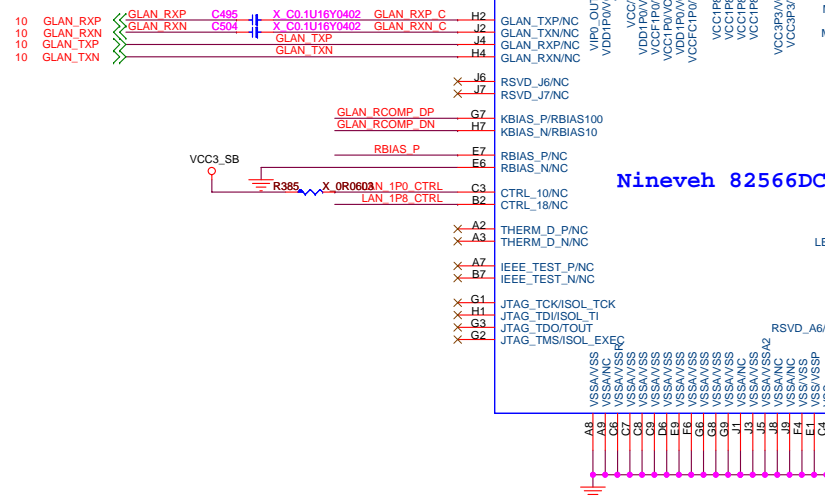
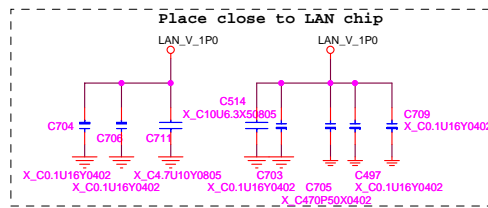


EMI SUGGESTION

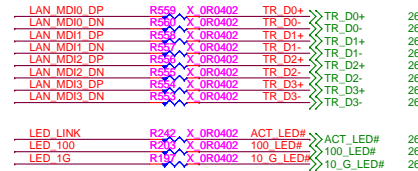
EMI SUGGESTION



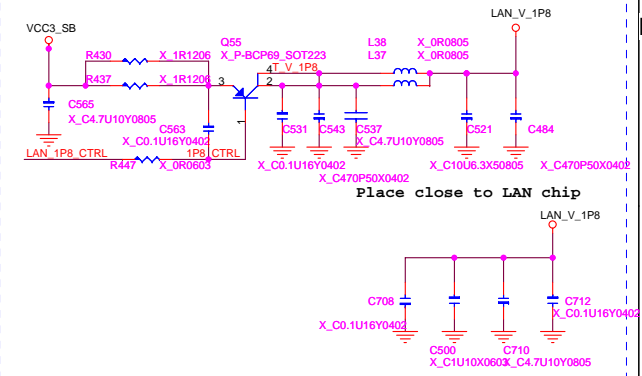
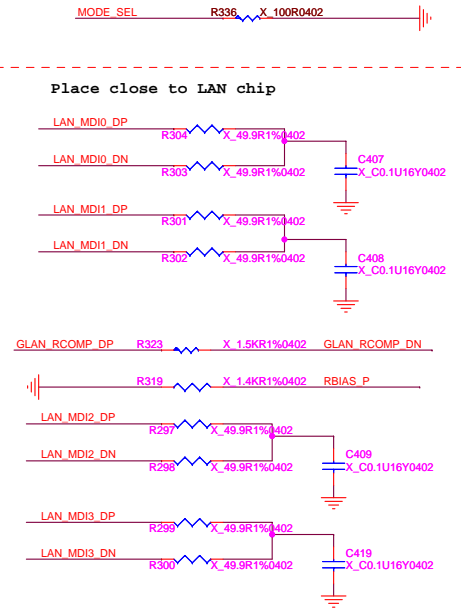
(ROPROS-VS USE)



LAN CONNECTOR



ACT_LED	Link_LED
S0: LOW	S0: LOW
S1/S3/S4/S5: HIGH	S5: HIGH
	S1/S3/S4: WOL EN-->LOW WOL DIS-->HIGH



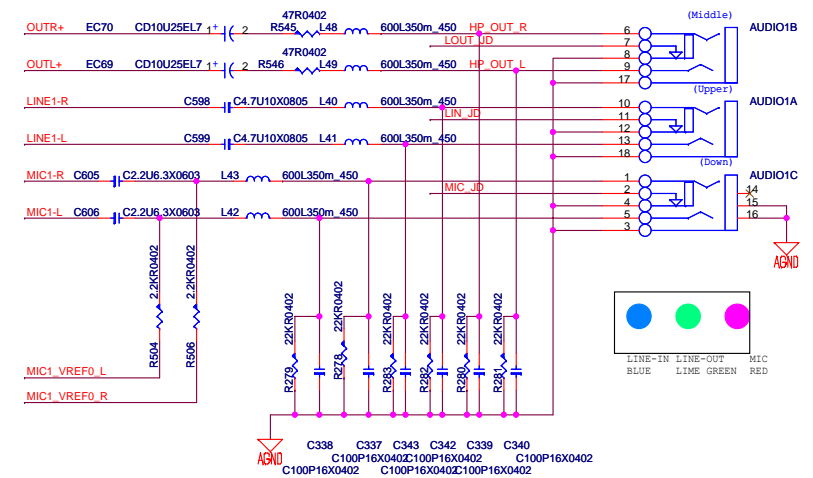
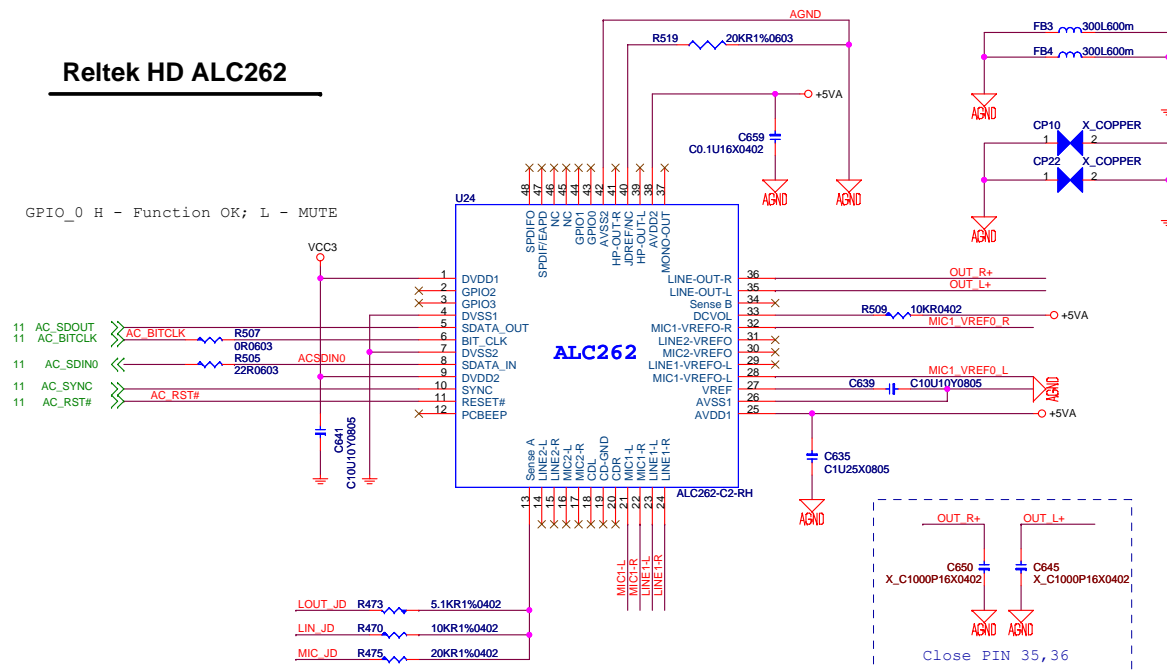
MICRO-STAR INT'L CO.,LTD

MS-7410

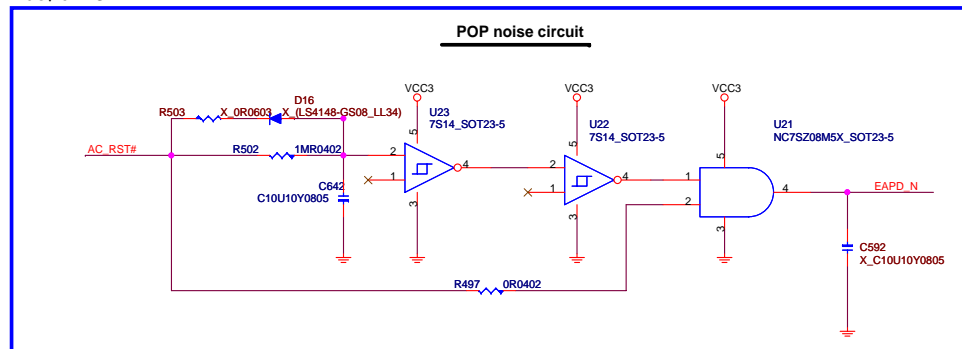
Size Custom	Document Description LAN-NINEVEH 82566	Rev 0B
Date: Wednesday, September 26, 2007		Sheet 27 of 34

Reltek HD ALC262

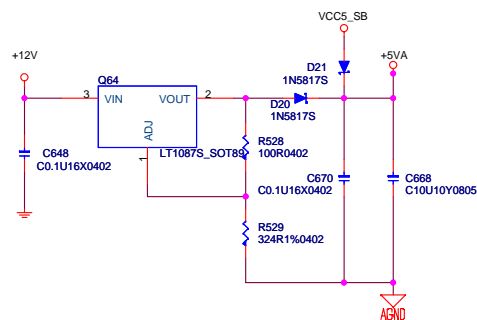
GPIO_0 H - Function OK; L - MUTE



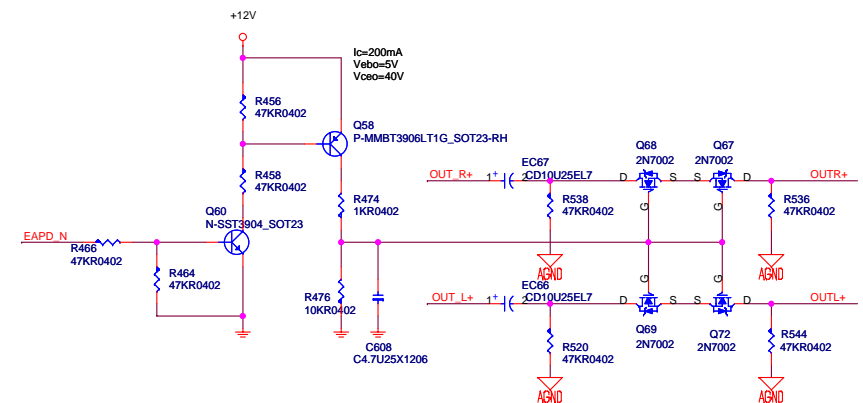
08/01 UPDATE



AUDIO CODE REGULATORS



Smooth pop noise circuit for Line-out



MICRO-STAR INT'L CO.,LTD

MS-7410

Size Custom	Document Description HD Audio ALC262	Rev 0B
Date: Wednesday, September 26, 2007	Sheet 28 of 34	

ICH9

GPIO	Alt Func	Pin	I/O/NC	Power	PÜ	Tol	Default	Signal Name or condition	
GPIO[0]	ATADET0	N7	I/O	Vcc3	Y	3.3	INPUT	ATADET0	PULL HIGH 10K
GPIO[1]	PULL HIGH	AK21	I/O	Vcc3	Y	3.3	INPUT	PULL HIGH	10K
GPIO[2]	PIRQ#E	K6	I/O	Vcc3	Y	3.3	INPUT	PULL HIGH	8.2K
GPIO[3]	PIRQ#F	L7	I/O	Vcc3	Y	3.3	INPUT	PULL HIGH	8.2K
GPIO[4]	PIRQ#G	F2	I/O	Vcc3	Y	3.3	INPUT	PULL HIGH	8.2K
GPIO[5]	PIRQ#H	G2	I/O	Vcc3	Y	3.3	INPUT	PULL HIGH	8.2K
GPIO[6]	PULL HIGH	AH22	I/O	Vcc3	Y	3.3	INPUT	PULL HIGH	10K
GPIO[7]	PULL HIGH	AK23	I/O	Vcc3	Y	3.3	INPUT	PULL HIGH	10K
GPIO[8]	ICH GP8 PU	A20	I/O	Vcc3SB	Y	3.3	INPUT	PULL HIGH	10K
GPIO[9]	SIO SMI#	A18	NC	Vcc3	N	3.3	WOL EN	NC	
GPIO[10]	ICH GP10 PU	C17	I/O	Vcc3SB	Y	3.3	INPUT	PULL HIGH	10K
GPIO[11]	SMB ALERT#	C16	I/O	Vcc3SB	Y	3.3	SMB ALERT#	PULL HIGH	10K
GPIO[12]	NC	A8	NC	Vcc3SB	N	3.3	OUTPUT	SIO SMI#	
GPIO[13]	SIO PME#	A19	I/O	Vcc3SB	Y	3.3	INPUT	SIO PME#	
GPIO[14]	CLR PW	A9	I/O	Vcc3SB	Y	3.3	INPUT	PULL HIGH	10K
GPIO[15]	NC	C15	NC	Vcc3SB	Y	3.3	STP PCI#	NC	
GPIO[16]	NC	M2	NC	Vcc3	Y	3.3	OUTPUT	NC	
GPIO[17]	PULL HIGH	AH21	I/O	Vcc3	Y	3.3	INPUT	PULL HIGH	10K
GPIO[18]	NC	K1	NC	Vcc3	N	3.3	OUTPUT	NC	
GPIO[19]	SATA1GP PU	AE20	I/O	Vcc3	Y	3.3	INPUT	PULL HIGH	10K
GPIO[20]	NC	AF5	NC	Vcc3	N	3.3	OUTPUT	NC	
GPIO[21]	SATA0GP PU	AK25	I/O	Vcc3	Y	3.3	INPUT	PULL HIGH	10K
GPIO[22]	ICH SGP22 PU	AJ24	I/O	Vcc3	Y	3.3	INPUT	PULL HIGH	10K
GPIO[23]	LDRQ 1#	J3	I/O	Vcc3	Y	3.3	LDRQ 1#	PULL HIGH	10K
GPIO[24]	LPM LAN	A14	NC	Vcc3SB	N	3.3	OUTPUT	LPM LAN	
GPIO[25]	NC	B18	NC	Vcc3SB	N	3.3	STP CPU#	NC	
GPIO[26]	NC	C11	NC	Vcc3SB	N	3.3	S4 STATE#	NC	
GPIO[27]	NC	A11	NC	Vcc3SB	N	3.3	QRT STATE0	NC	
GPIO[28]	NC	G18	NC	Vcc3SB	N	3.3	QRT STATE1	NC	
GPIO[29]	USB OC#2	N1	I/O	Vcc3SB	Y	3.3	OC#2	USB OC#2	
GPIO[30]	USB OC#3	N5	I/O	Vcc3SB	Y	3.3	OC#3	USB OC#3	
GPIO[31]	USB OC#3	M1	I/O	Vcc3SB	Y	3.3	OC#3	USB OC#3	
GPIO[32]	SPI WP#	K2	I/O	Vcc3	N	3.3	OUTPUT	SPI WP#	
GPIO[33]	SPI HOLD GPO#	AF6	I/O	Vcc3	N	3.3	OUTPUT	SPI HOLD GPO#	
GPIO[34]	LAN DISABLE	AH5	I/O	Vcc3	N	3.3	OUTPUT	LAN DISABLE	
GPIO[35]	NC	L1	NC	Vcc3	N	3.3	OUTPUT	NC	
GPIO[36]	SATA2GP PU	AE21	I/O	Vcc3	Y	3.3	INPUT	SATA2GP PU	
GPIO[37]	SATA3GP PU	AE22	I/O	Vcc3	Y	3.3	INPUT	SATA3GP PU	
GPIO[38]	ICH SGP38 PU	AK24	I/O	Vcc3	Y	3.3	INPUT	ICH SGP38 PU	
GPIO[39]	ICH SGP39 PD	AH23	I/O	Vcc3	Y	3.3	SDATAOUT0	ICH SGP39 PD	
GPIO[40]	USB OC#0	N3	I/O	Vcc3SB	Y	3.3	OC#0	USB OC#0	
GPIO[41]	USB OC#1	P7	I/O	Vcc3SB	Y	3.3	OC#1	USB OC#1	
GPIO[42]	USB OC#1	R7	I/O	Vcc3SB	Y	3.3	OC#1	USB OC#1	
GPIO[43]	USB OC#2	N2	I/O	Vcc3SB	Y	3.3	OC#2	USB OC#2	
GPIO[44]	USB OC#3	P3	I/O	Vcc3SB	Y	3.3	OC#3	USB OC#3	
GPIO[45]	USB OC#3	R6	I/O	Vcc3SB	Y	3.3	OC#3	USB OC#3	
GPIO[46]	USB OC#3	T7	I/O	Vcc3SB	Y	3.3	OC#3	USB OC#3	
GPIO[47]	USB OC#3	P1	I/O	Vcc3SB	Y	3.3	OC#3	USB OC#3	
GPIO[48]	ICH SGP48 PD	AD20	I/O	Vcc3	Y	3.3	SDATAOUT1	PULL HIGH	10K
GPIO[49]	DMI STRAP	AJ25	I/O	Vcc3	N	3.3	OUTPUT	PULL LOW	2.2K
GPIO[50]	PREQ#1	G13	I/O	Vcc5	Y	5.5	PREQ#1	PULL HIGH	2.7K
GPIO[51]	PGNT#1	A7	I/O	Vcc3	N	3.3	PGNT#1	PGNT#1	
GPIO[52]	PREQ#2	F13	I/O	Vcc5	Y	5.5	PREQ#2	PULL HIGH	2.7K
GPIO[53]	PGNT#2	C7	I/O	Vcc3	N	3.3	PGNT#2	STRAP PIN	
GPIO[54]	PREQ#3	G8	I/O	Vcc5	Y	5.5	PREQ#3	PULL HIGH	2.7K
GPIO[55]	PGNT#3	F7	I/O	Vcc3	N	3.3	PGNT#3	STRAP PIN	
GPIO[56]	ICH GP56 PU	F16	I/O	Vcc3SB	Y	3.3	GPIO SEL	PULL HIGH	10K
GPIO[57]	ICH GP57 PU	C12	I/O	Vcc3SB	Y	3.3	INPUT	PULL HIGH	10K
GPIO[58]	SPI CS1#	F23	I/O	Vcc3SB	Y	3.3	SPI CS1#	SPI CS1#	
GPIO[59]	USB OC#0	P5	I/O	Vcc3SB	Y	3.3	OC#0	USB OC#0	
GPIO[60]	LINK ALERT#	F18	I/O	Vcc3SB	Y	3.3	LINK ALERT#	LINK ALERT#	

SIO SCH5617

PIN NAME	PIN#	USAGE	Input/Output
GP76	53	GPIO_KB	OUTPUT
GP42	27	SIO_SMI#	OUTPUT
GP41	77	SIO_PME#	OUTPUT

PCI Config.

DEVICE	MCP1 INT Pin	REQ#/GNT#	IDSEL	CLOCK
PCI1	PIRQ#A PIRQ#B PIRQ#C PIRQ#D	PREQ#0 PGNT#0	AD16	PCI_CLK0
PCI2	PIRQ#B PIRQ#D PIRQ#C PIRQ#A	PREQ#1 PGNT#1	AD17	PCI_CLK1

DDRII DIMM Config.

DEVICE	ADDRESS	CLOCK
DIMM 1	A0H	MCLK_A0/MCLK_A#0 MCLK_A1/MCLK_A#1 MCLK_A2/MCLK_A#2
DIMM 2	A2H	MCLK_A1/MCLK_A#3 MCLK_A2/MCLK_A#4 MCLK_A2/MCLK_A#5
DIMM 3	A4H	MCLK_B0/MCLK_B#0 MCLK_B2/MCLK_B#1 MCLK_B1/MCLK_B#2
DIMM 4	A6H	MCLK_B0/MCLK_B#3 MCLK_B1/MCLK_B#4 MCLK_B2/MCLK_B#5

JUMPER SETTING

JBAT1	(1-2) NORMAL	(2-3) CLEAR
--------------	--------------	-------------



MICRO-STAR INT'L CO.,LTD			
MS-7410			
Size Custom	Document Description GPIO & Jumper setting		Rev 0B
Date: Wednesday, September 26, 2007		Sheet 29 of 34	

MANUAL PART



JBAT1(1-2)1
JMP/GREEN/A



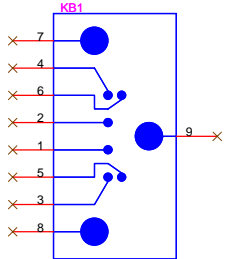
BATTERY HOLDER, 2PIN



REPOS-NECCAP

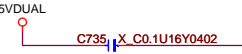
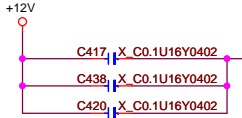
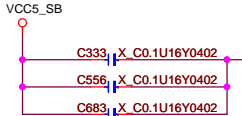
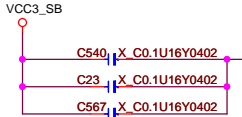
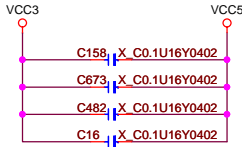
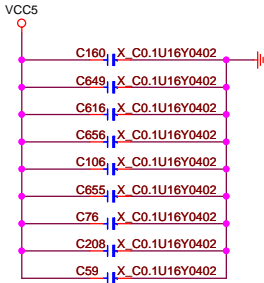
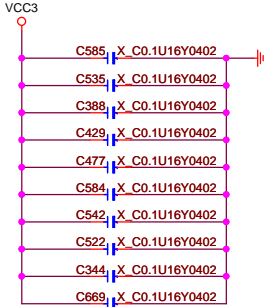
U18_R
INTEL
ICH9R
X_INTEL_ICH9R

REPOS-VS



PURPLE
X_MINIDIN-D6-ML
U18_DH
INTEL
ICH9 DH
X_INTEL_ICH9DH

EMI SUGGESTION



Model option table

Model type	Function	BOM Config	ERP BOM No.
MS7410-MA	INTEL G33 + ICH9 + Broadcom Giga Lan		
MS7410-VS	INTEL G33 + ICH9DH + Intel 82566 Giga Lan		
MS7410-NECCAP	INTEL G33 + ICH9R + Broadcom Giga Lan		



MICRO-STAR INT'L CO.,LTD

MS-7410

Size Custom Document Description
MANUAL PARTS

Rev 0B

CedarMill / Smithfield		
0.8375V - 1.6000V Core	-	100A
1.2V FSB Vtt	-	5.3A

Bearlake-Q		
1.2V FSB_VTT	-	1.3 A
1.25V Core	-	18.8A
1.25V DMI/PCI Exp.	-	2.5 A
1.8V VCC_DDR (S0,S1)	-	3.73A
1.8V VCC_SMCLK	-	TBD
3.3V VCCA_DAC	-	66 mA
3.3V VCC33	-	15.8mA
1.25V Vcc CL	-	4.24A

ICH9		
1.05V Core	-	1.17A
1.25V DMI	-	40 mA
1.2V FSB_VTT	-	14 mA
1.5V_A USB/SATA	-	1.12A
1.5V_B PCI Exp.	-	0.77A
VCCRTC	-	6 uA
3.3V CL	-	12 mA
1.5V GbE LAN	-	74 mA
3.3V 10/100 LAN	-	12 mA
3.3V GbE LAN	-	1 mA
3.3V SusHDA	-	4 mA
3.3V HDA	-	24 mA

HD Audio ALC662		
3.3V AUDIO	-	40mA
5V AUDIO	-	200mA

CK505		
3.3V VDD 48/PCI/REF	-	TBDA
0.3V - 1V CPU/SRC/DOT/PLL	-	TBDA

BCM5786		
3.3V_SB I/O & LED	-	15.5mA
2.5V ANALOG	-	0.418A

ISL6312		
VCCP	VRM 11	
0.8375V-1.6000V	85A	
3-Phase Switch		

W83310DS		
VTT_DDR		
0.9V Linear	2A	

MS11+ Regulator		
VCC_DDR		
1.8V PWM	15A	

MS7 Regulator		
V_1P25_CORE		
1.25V PWM	21.34A	
V_1P25_CL		
1.25V Linear	4.24A	
V_FSB_VTT		
1.2V Linear	6.2A	
V_1P5_ICH	2A	
1.5V Linear		
V_1P05_ICH		
1.05V Linear	2 A	
VCC3_SB		
3.3V Linear	1.5A	
5V Dual	5A	
5VSB Switch	500mA	
5V DIMM	15A	
5VSB Switch	500mA	

DDRII x4 & TERMINATOR		
0.9V VTT_DDR	-	1.2A
1.8V VCC_DDR (S0,S1)	-	9.4A
1.8V VCC_DDR (S3)	-	400mA

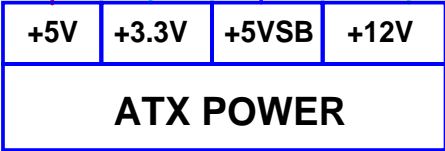
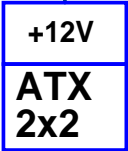
PCI Express x16 slot		
+12V	-	5.5 A
+3.3Vaux (wake)	-	375mA
+3.3Vaux (no wake)	-	20mA
+3.3V	-	3.0A

PCI slot x1		
+3.3Vaux (wake)	-	375mA
+3.3Vaux (no wake)	-	20mA
+3.3V	-	7.6A
+5V	-	5.0A
+12V	-	0.5A

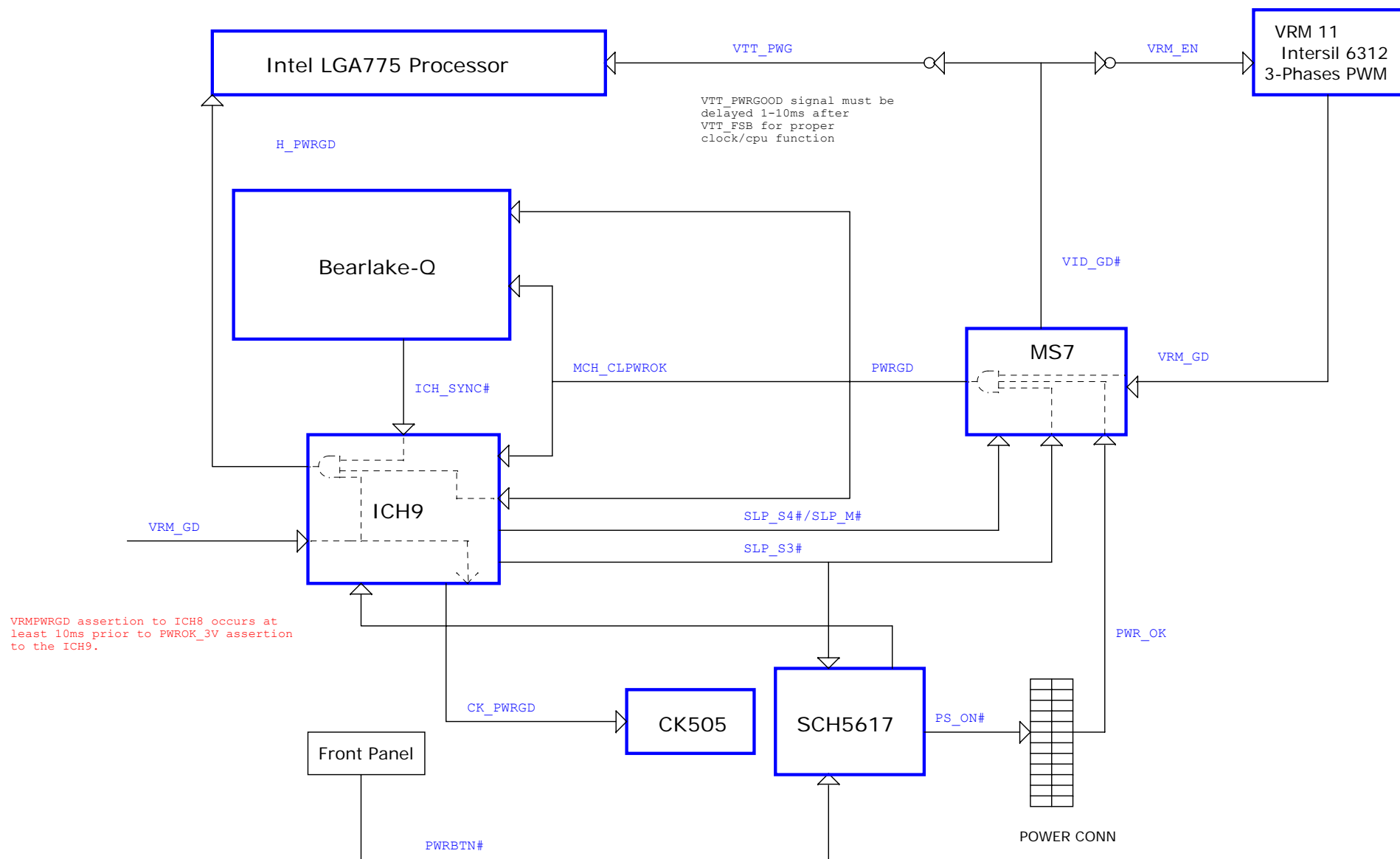
PCI Express x 1 slot *2		
+12V	-	0.5 A
+3.3Vaux (wake)	-	375mA
+3.3Vaux (no wake)	-	20mA
+3.3V	-	3.0A

USB x12		
+5V (S0,S1)	-	6.0A
+5V (S3)	-	20mA

PS2		
+5V (S0,S1)	-	345mA
+5V (S3)	-	2.0mA



PWROK MAP

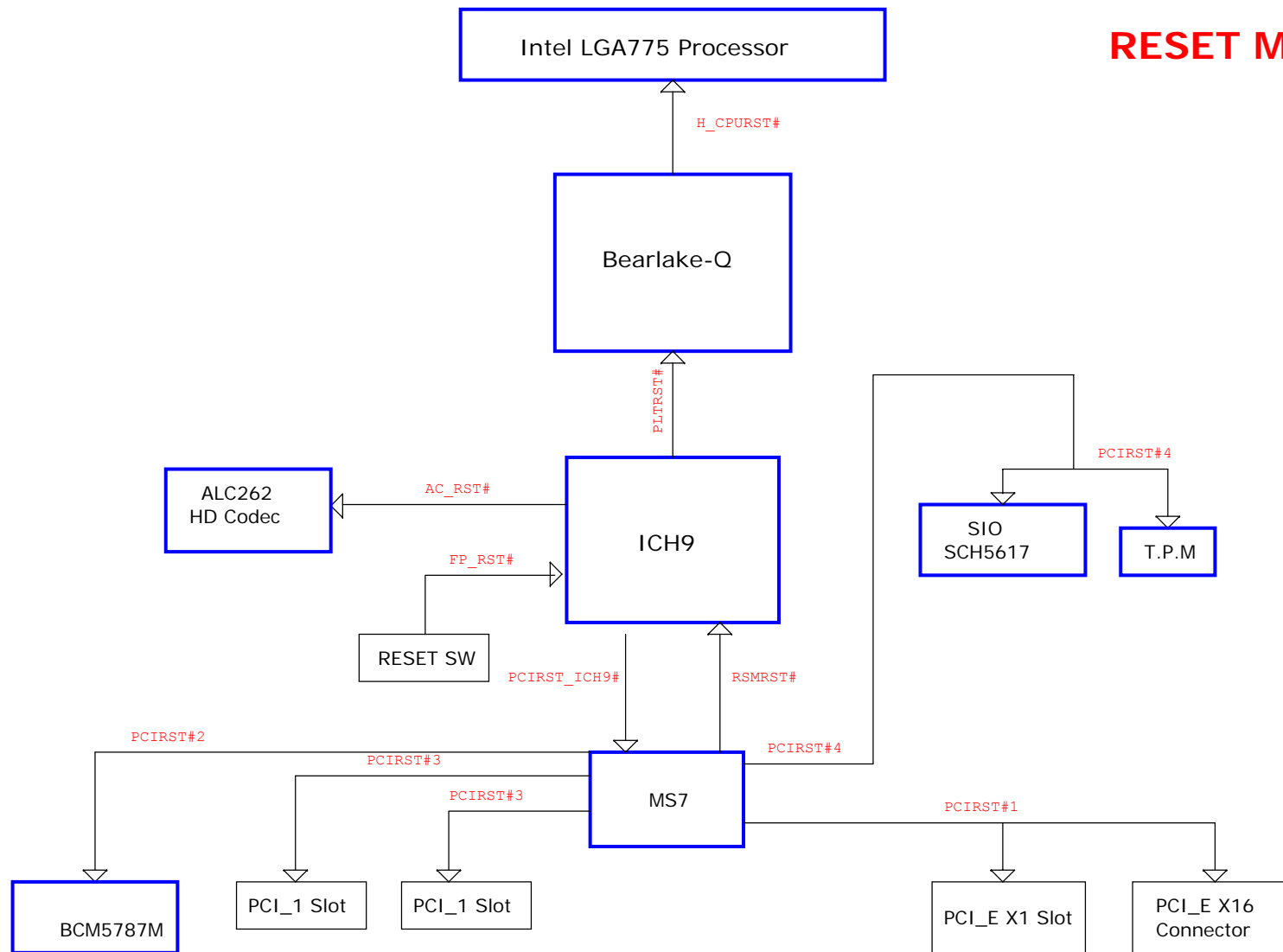


MICRO-STAR INT'L CO.,LTD

MS-7410

Size	Document Description	Rev
Custom	PWROK MAP	0B
Date: Wednesday, September 26, 2007	Sheet 32 of 34	

RESET MAP



MICRO-STAR INT'L CO.,LTD

MS-7410


Size Custom	Document Description RESET MAP	Rev 0B
Date: Wednesday, September 26, 2007		Sheet 33 of 34

Change Note

Ver:0A

2007/09/06

- 1.PAGE 4:Add R561 C721 Q73 for VTT SEL control circuit
- 2.PAGE 11:change the net name of SATA2.3&SATA4.5 to avoid confuse
- 3.PAGE 11: add R564 pull-down resister to LAN_PWROK ,when not use intel lan ,the LAN_PWROK need tied to gnd
- 4.PAGE 12: To change the net of VccCL3_3&VccLAN3_3 power source form VCC3 to VCC3_SB for INTEL LAN W/O F/T
- 5.PAGE 20:Front_USB1&Front_USB2 PIN5 tied to gnd for MCR Device use
- 6.PAGE 22:change VCC5_MS power rail to 5VDUAL to avoid MS have voltage when enter S5 state
- 7.PAGE 24:change VTT_SEL control circuit to follow up 7400 design
- 8.PAGE10& PAGE20:change USB PORT from6&7 port to 10&11 port
- 9.PAGE23:remove EC18 ,add EC76~EC81 for CPU power quility



MICRO-STAR INT'L CO.,LTD		
MS-7410		
Size B	Document Description History	Rev 0B
Date: Wednesday, September 26, 2007		Sheet 34 of 34